C141-C007-01EN

MAT3073, MAT3147, MAT3300 NP/NC SERIES
MAU3036, MAU3073, MAU3147 NP/NC SERIES
DISK DRIVES

SCSI PHYSICAL INTERFACE SPECIFICATIONS

FUJITSU

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There may be certain functional limitations concerning the specifications and functions of the products covered by this manual depending on the equipment version, especially concerning the following functions.

Versions in which there functions can be used will be communicated through “ENGINEERING CHANGE REQUEST/NOTICE”, issued by Fujitsu.

Function	Equipment Version Which Supports These Functions		
	Equipment Version No.	EPROM Version No.	Standard INQUIRY Data Product Revision (ASCII)
WRITE RAM Command READ RAM Command	These commands cannot be used in the current version.		

(Proceed to the Copyright Page)

Related Standards

Specifications and functions of products covered by this manual comply with the following standards.

Standard (Text) No.	Name	Enacting Organization
T10/1365D Rev 10	Working Draft American National Standard Information Technology --- SCSI Parallel Interface 4	American National Standards Institute (ANSI)

REVISION RECORD		
Edition	**Date published**	**Revised contents**
01	**Mar.,2004**	**Initial release**
Specification No.: C141-C007		

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PREFACE

This manual explains the MAT3073/MAT3147/MAT3300/MAU3036/MAU3073/MAU3147 NP/NC series 3-1/2" intelligent disk drives each having the built-in SCSI controller.

This manual details the specifications and functions of the Small Computer System Interface (SCSI) to connect the above listed disk drives to the user system. Also, the manual details various SCSI command specifications and the command processing functions, and provides the information required to creation of host system software. This manual is intended to be used by the users who have the basic knowledge of computer system operations.

The following lists the manual configuration and the contents of each chapter. The caution labels and markings are also explained.

Manual Configuration and Contents

This manual consists of the following three chapters, and the terminologies and abbreviations sections.

Chapter 1 SCSI Bus

This chapter describes the configuration, physical and electrical requirements, interface protocol, and other operations of the Small Computer System Interface (SCSI) which connects the MAT3073/MAT3147/MAT3300/MAU3036/MAU3073/MAU3147 NP/NC series intelligent disk drives to the user system.

Chapter 2 SCSI Messages

This chapter describes the type and explanation of messages defined for SCSI bus operations.

Chapter 3 ERROR Recovery

This chapter describes error recovery processing executed by the MAT3073/MAT3147/MAT3300/ MAU3036/MAU3073/MAU3147 NP/NC series intelligent disk drives in response to various errors on the SCSI bus.

Glossary

This section explains the terminologies the reader must understand to read this manual.

Abbreviations

This section lists the abbreviated terms and their full words used in this manual.

CONVENTIONS

This manual uses the following conventions:

NOTE: NOTE indicates the information useful for the user to operate the system.

Important information

The important information is provided with the "Important" title. The important information text is centered so that the reader can distinguish it from other manual texts. The following gives an example:

IMPORTANT

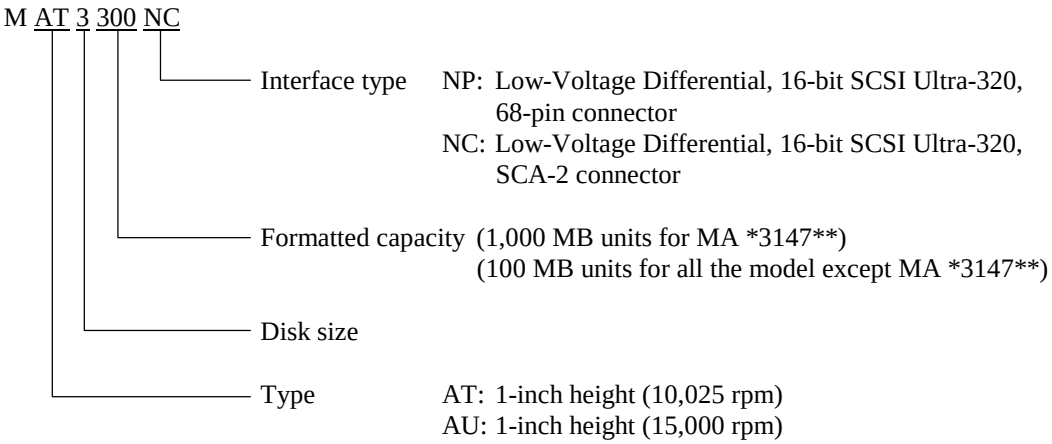
The IDD operates as a target (TARG) on the SCSI bus. The IDD is called "TARG" in this chapter except when clear identification is required.

Notations

A decimal value is indicated as it is in this manual.
A hexadecimal value is indicated in the X'17B9' or 17B9h or 17B9H notation.
A binary value is indicated in the notation similar to "010."

The disk drive model name has a different suffix depending on its SCSI electrical characteristics, capacity, data format used during shipment and others. The following typical model name is used except when the model needs to be distinguished. Also, the disk unit may be referred to as the "IDD" or "unit" in this manual.

Note 1: Model name



Note 2: Typical model name

Type model name	Model name
MAT3300	MAT3300NP, MAT3300NC
MAT3147	MAT3147NP, MAT3147NC
MAT3073	MAT3073NP, MAT3073NC
MAU3147	MAU3147NP, MAU3147NC
MAU3073	MAU3073NP, MAU3073NC
MAU3036	MAU3036NP, MAU3036NC

Requesting for User's Comments

Please use the User's Comment Form attached to the end of this manual to identify user comments including error, inaccurate and misleading information of this manual. Contact to your Fujitsu representative for additional comment forms if required.

MANUAL ORGANIZATION

Product/ Maintenance Manual	• General Description • Specifications • Data Format • Installation Requirements • Installation • Diagnostics and Maintenance • Error Analysis • Principle of Operation
SCSI Physical Interface Specifications	• SCSI Bus • SCSI Message • Error Recovery
SCSI Logical Interface Specifications	• Command Processing • Data Buffer Management • Command Specifications • Parameter Data Formats • Sense Data and Error Recovery Methods • Disk Media Management

CONTENTS

page

FIGURES

TABLES

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CHAPTER 1 SCSI BUS

This chapter describes the configuration, physical and electrical characteristics, interface protocol, and operations of SCSI buses.

Note:

The IDD operates as a target (TARG) on the SCSI bus. The IDD is called "TARG" in this chapter except when clear identification is required.

1.1 System Configuration

Up to 16-bit SCSI series models can be connected to the system via the SCSI bus. Figure 1.1 gives an example of multi-host system configuration.

Each SCSI device operates as an initiator (INIT) or a target (TARG). Only a single INIT and a single TARG selected by this INIT can operate simultaneously on the SCSI bus.

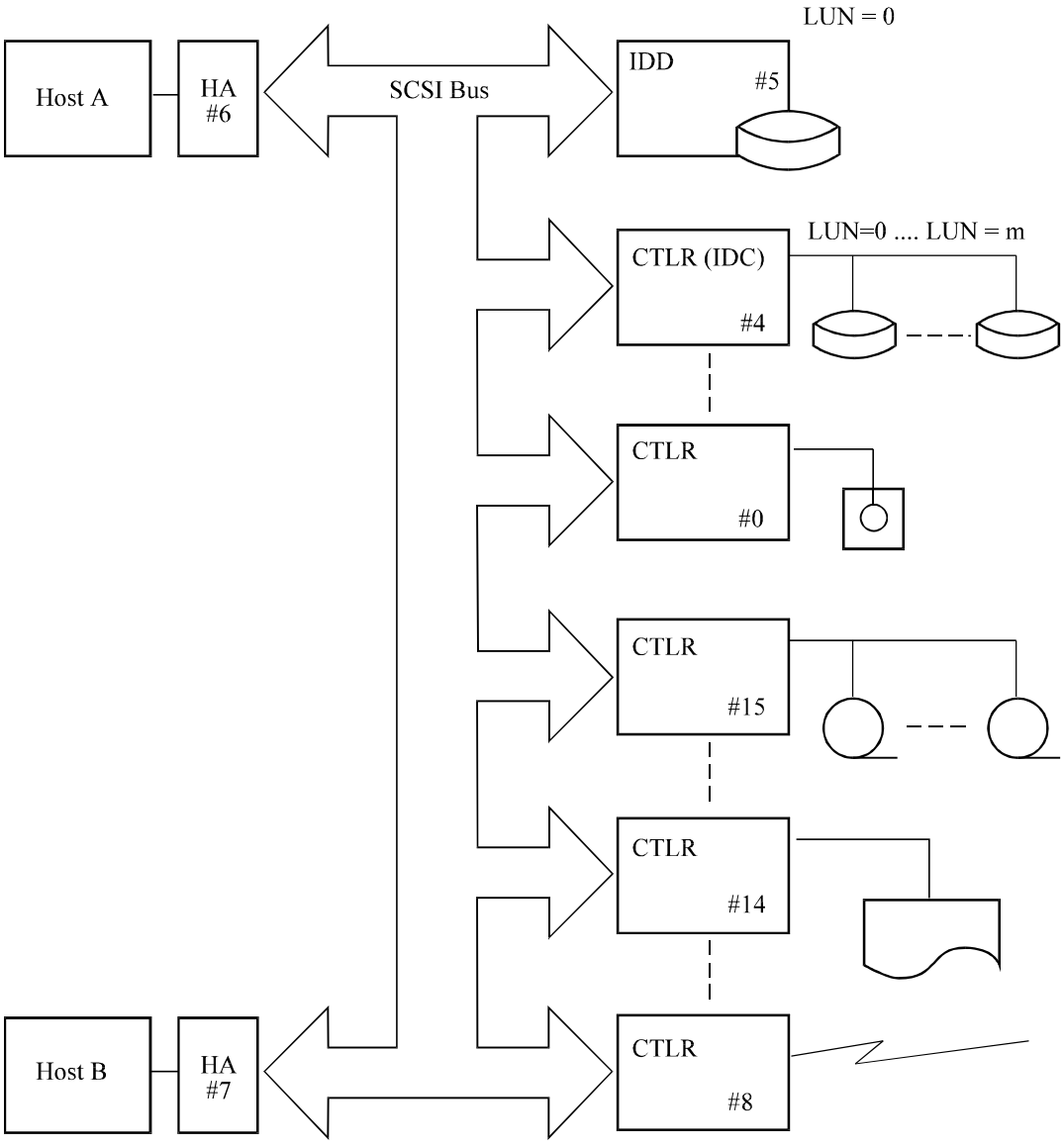
The system configuration allows any combination of a SCSI device to operate as the INIT and a SCSI device to operate as the TARG. Also, any device having both the INIT and TARG functions can be used on the SCSI bus.

Each SCSI device is assigned a unique address (or SCSI ID). The SCSI ID corresponds to a bit number of the SCSI data bus. While the INIT uses a logical unit number (LUN) to select an I/O unit to be connected under TARG control.

Any SCSI ID of the IDD can be selected using the setup pins. However, the LUN is fixed to zero (0). The SCSI ID can be 0 to 15.

Note:

The maximum number of SCSI devices and the maximum cable length are limited depending on the selected SCSI data transfer mode and the SCSI transceiver type. Appropriate SCSI devices and cable length must be determined for each system.



#n : SCSI ID, HA: Host adapter

Figure 1.1 Example of SCSI configuration

1.2 Interface Signal Definition

Figure 1.2 shows interface signal types. The SCSI bus consists of 27 signal lines. The 27 signal lines consist of data buses (2 bytes plus two odd parity bits) and 9 control signal lines.

The SCSI bus can be a single-ended or low voltage differential(LVD) interface depending on the model used. Their physical and electrical characteristics are detailed in Sections 1.3 and 1.4.

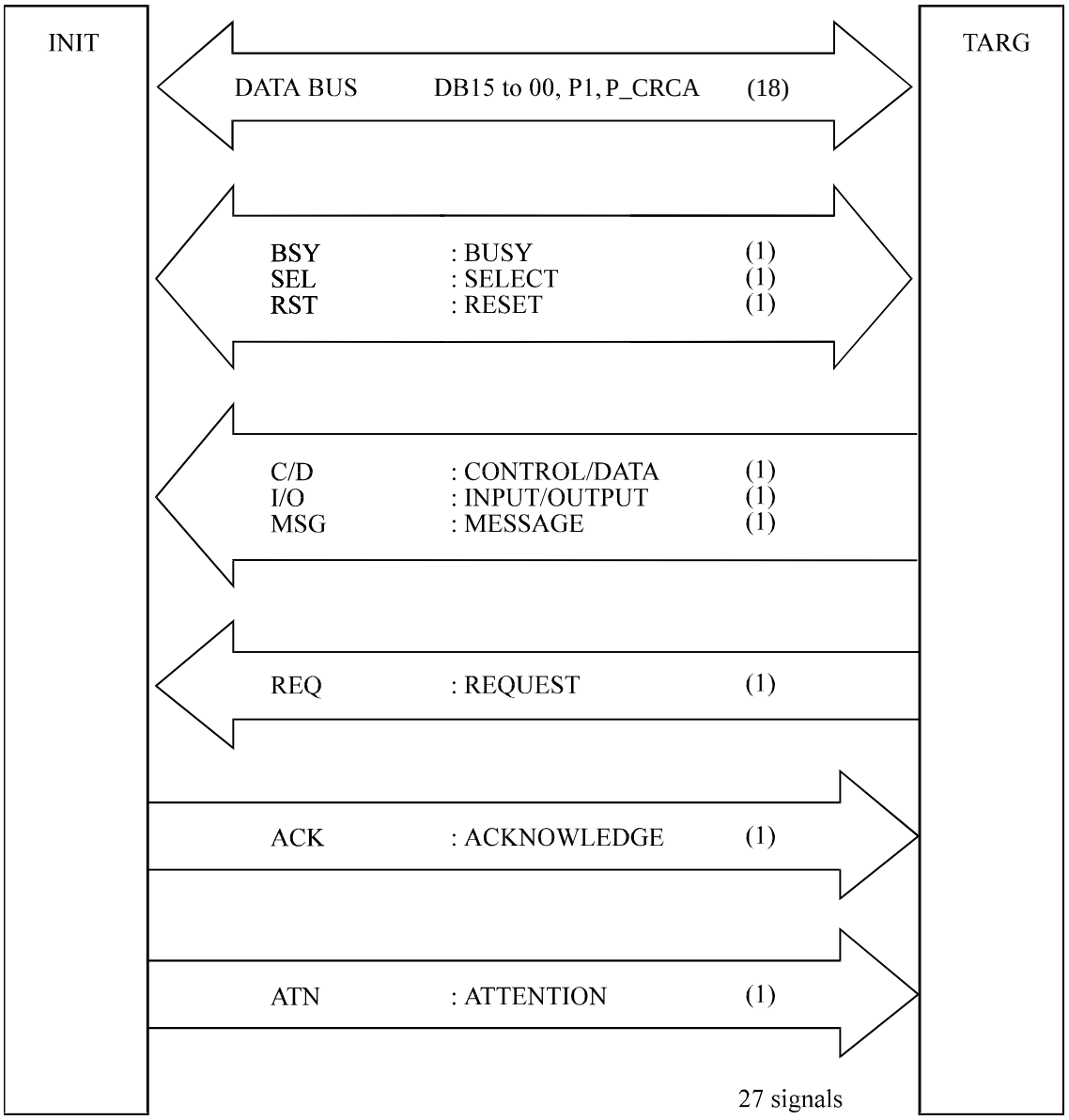


Figure 1.2 Interface signals

(1) DB15 to DB00, P1, P_CRCA (Data buses)

The 16-bit SCSI system uses a bidirectional data bus consisting of two-byte data and two odd parity bits.

MSB (2^{15}): DB15, LSB (2^{0}): DB00

The data bus is used to transfer a command, data, a status, or a message in the INFORMATION TRANSFER phase. However, DB15 to DB08 and P1 are used for data transfer only. The data is transferred only after the WIDE DATA TRANSFER REQUEST or PARALLEL PROTOCOL REQUEST message has been exchanged and the 16-bit data transfer mode has been established between the INIT and TARG.

In the ARBITRATION phase, the data bus is used to send a SCSI ID to determine the bus arbitration priority. In the SELECTION or RESELECTION phase, the data bus is used to send a SCSI ID of the INIT and TARG. Figure 1.3 shows the relationship between the data buses and SCSI IDs.

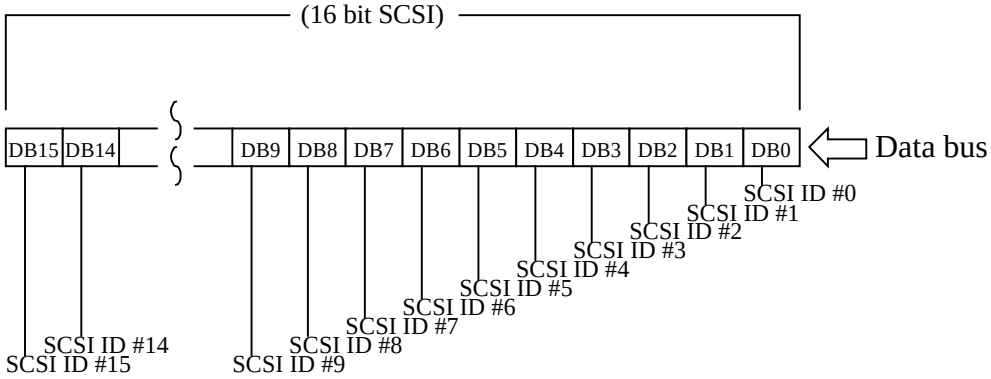


Figure 1.3 DATA BUS and SCSI ID

(a) DB15 to 0

Sixteen data-bit signals that form the 16-bit DATA BUS.

(b) DB7 to 0

Eight data-bit signals that form the 16-bit DATA BUS.

(c) P1 (ST DATA phase)

A signal sourced by the SCSI device driving the data bus during ST DATA phases. This signal is associated with the DB(15-8) signals and is used to detect the presence of an odd number of bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is odd.

(d) P1 (data group transfer enabled)

A signal that shall be continuously negated by the SCSI device driving the DB(15-0) signals and shall be ignored by the SCSI device receiving the DB(15-0) signals during DT DATA phases.

(e) PI (information unit and paced transfer enabled)

A signal that is sourced by SCSI device to indicate the data valid or data invalid state.

(f) P_CRCA (PARITY/CRC AVAILABLE) (SELECTION phase, ST DATA phase, COMMAND phase, MESSAGE phase, or STATUS phase)

A signal sourced by the SCSI device driving the data bus during these phases. This signal is associated with the DB(7-0) signals and is used to detect the presence of an odd number of bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is odd.

The parity bits (P1 and P_CRCA) is optional for the system. The IDD handles the data bus parity as follows:

- The IDD has the data bus parity check function, and can enable or disable the parity check. See Section 5.3.2 "SCSI Parity" of the Product Manual for setup details.
- When valid data is sent to the data bus from the IDD, the parity data is always guaranteed except for the ARBITRATION phase.

(g) P_CRCA (data group transfer enabled)

A signal sourced by a target during DT DATA phases to control whether a data group field is a pad field, pCRC field, or data field. When asserted the data group field shall be pad or pCRC fields that shall not be transferred to the ULP. When negated the data group field shall be a data field that shall be transferred to the ULP.

Note:

ULP is "Upper Level Protocol".

(h) P_CRCA (information unit and paced transfer enabled)

During DT DATA phases when information unit transfers are enabled this signal is referred to as P_CRCA and is sourced by the SCSI target port. Depending on the negotiated condition of read streaming and write flow control the SCSI initiator port and SCSI target port usage for P_CRCA is different. When information unit transfers are enabled the SCSI target port and SCSI initiator port shall use the P_CRCA signal.

(2) BSY (BUSY)

The BSY signal indicates that the SCSI bus is in use. In the ARBITRATION phase, this signal is used to request for the bus usage priority.

(3) SEL (SELECT)

The SEL signal is used by the INIT to select a TARG (in the SELECTION phase) or by the TARG to reselect an INIT (in the RESELECTION phase).

(4) C/D (CONTROL/DATA)

This is a combination of I/O and MSG signals, and specifies a type of information transferred on the data bus. The C/D signal is always driven by the TARG (see Table 1.1).

(5) I/O (INPUT/OUTPUT)

The I/O signal specifies the information transmission direction on the data bus. It is also used to identify the SELECTION phase or RESELECTION phase. This signal is always driven by the TARG (see Table 1.1).

(6) MSG (MESSAGE)

A signal sourced by a target to indicate the MESSAGE phase or a DT DATA phase depending on whether C/D is true or false. Asserted indicates MESSAGE or DT DATA (see Table 1.1).

Table 1.1 INFORMATION TRANSFER phase identification

Signal			Phase	Direction	Comment	
C/D	MSG	I/O				
0	0	0	ST DATA OUT	INIT -> TARG	ST Data phase	Data phase
0	0	1	ST DATA IN	INIT <- TARG		
0	1	0	DT DATA OUT	INIT -> TARG	DT Data phase	
0	1	1	DT DATA IN	INIT <- TARG		
1	0	0	COMMAND	INIT -> TARG		
1	0	1	STATUS	INIT <- TARG		
1	1	0	MESSAGE OUT	INIT -> TARG	MESSAGE	
1	1	1	MESSAGE IN	INIT <- TARG		

(7) REQ (REQUEST)

This is a transmission request from the TARG to the INIT in the INFORMATION TRANSFER phase.

(8) ACK (ACKNOWLEDGE)

The ACK signal is a response to the REQ signal sent from the INIT to TARG in the INFORMATION TRANSFER phase.

(9) ATN (ATTENTION)

The ATN signal indicates that the INIT has a message to be sent to the TARG. It is used to generate an ATTENTION condition.

(10) RST (RESET)

The RST signal is a Reset signal to clear all SCSI devices on the bus (to the RESET condition).

1.3 Physical Requirements

All SCSI devices are connected to each other in a daisy chain. Both ends of the interface cable are terminated with resistor.

Tables 1.2 and 1.3 define the SCSI bus electrical characteristics (for interface signal driver/receiver).

Table 1.2 Single-Ended maximum distance between terminators

Number of attached devices	Maximum distance between terminators (meters)		
	FAST-5	FAST-10	FAST-20
2 to 4 devices	6	3	3
5 to 8 devices	6	3	1.5
9 to 16 devices	6	3	N/A

Table 1.3 LVD maximum distance between terminators

Interconnect	Maximum distance between terminators (meters)					
	Fast-5	Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
Point-to-point	25	25	25	25	25	25
Multidrop	12	12	12	12	12	12

1.3.1 Interface connector

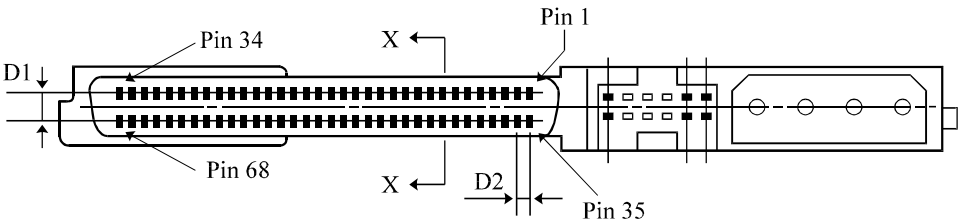
(1) Interface connector of the 16-bit SCSI

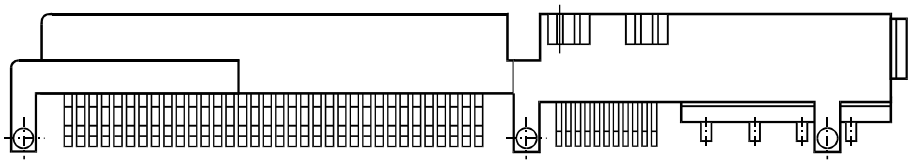
The IDD 16-bit SCSI bus connector is nonshielded 68-pin, consisting of two 34-pin rows with adjacent pins 1.27 mm (0.05 inch) part (Figure 1.4).

For the interface cable connector, use a nonshielded 68-contact socket consisting of two 34-contact rows points with adjacent contact points 1.27 mm (0.05 inch) apart (Figure 1.5).

Figure 1.6 shows single-ended interface connector signal assignment.

Figure 1.7 shows low-voltage-differential interface connector signal assignment.



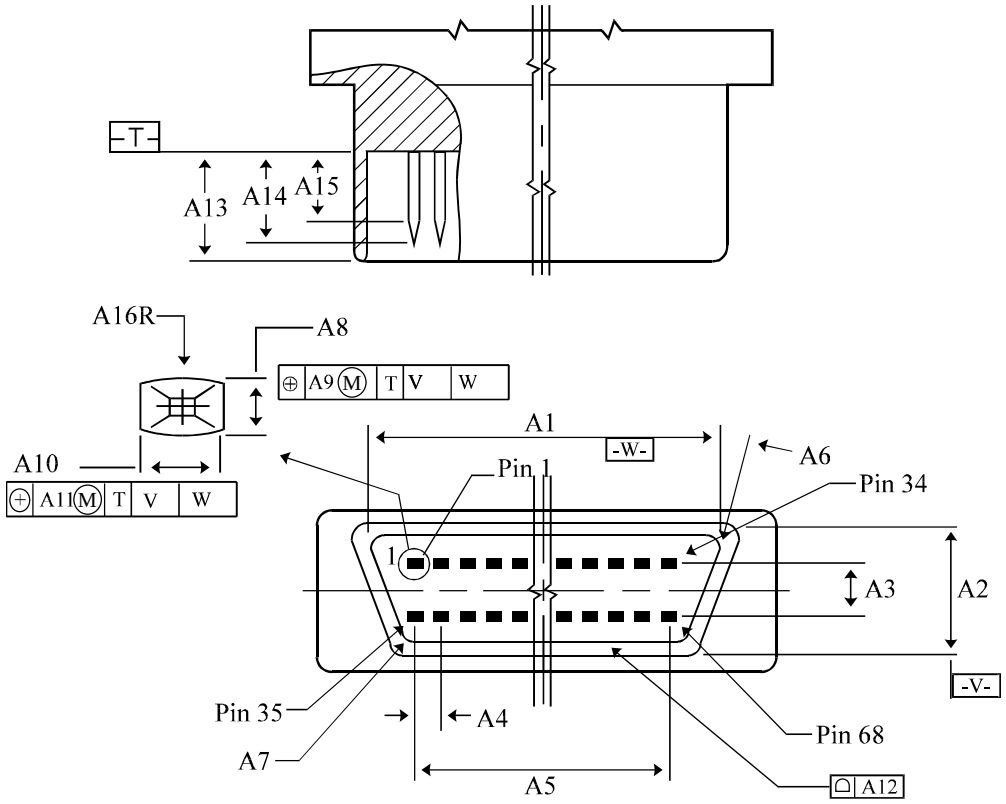


Symbol	mm	inch	Remarks
D1	2.54	0.100	
D2	1.27	0.050	

Note:

The tolerance is ±0.127 mm (0.005 inch) unless otherwise specified.

Figure 1.4 SCSI interface connector (IDD side) (16-bit SCSI)



Dimensions	68 position	
	Millimeters	Inches
A1	46.28	1.822
A2	5.69	0.224
A3	2.54	0.100
A4	1.27	0.050
A5	41.91	1.650
A6	15°	15°
A7	1.04R	0.041R
A8	0.396 ±0.010	0.0156±0.0004
A9	0.23	0.009
A10	0.61±0.03	0.024± 0.001
A11	0.23	0.009
A12	0.05	0.002
A13	5.16 ±0.15	0.203±0.006
A14	4.39 Max.	0.173 Max.
A15	3.02 Min.	0.119 Min.
A16	1.02±0.25	0.040±0.010

Figure 1.5 SCSI interface connector (cable side) (16-bit SCSI)

Pin No.	Signal	Signal	Pin No.
01	GND	-DB12	35
02	GND	-DB13	36
03	GND	-DB14	37
04	GND	-DB15	38
05	GND	-DBP1	39
06	GND	-DB00	40
07	GND	-DB01	41
08	GND	-DB02	42
09	GND	-DB03	43
10	GND	-DB04	44
11	GND	-DB05	45
12	GND	-DB06	46
13	GND	-DBP7	47
14	GND	-P_CRCA	48
15	GND	GND	49
16	GND	GND	50
17	TERMPWR *	TERMPWR *	51
18	TERMPWR *	TERMPWR *	52
19	(reserved)	(reserved)	53
20	GND	GND	54
21	GND	-ATN	55
22	GND	GND	56
23	GND	-BSY	57
24	GND	-ACK	58
25	GND	-RST	59
26	GND	-MSG	60
27	GND	-SEL	61
28	GND	-C/D	62
29	GND	-REQ	63
30	GND	-I/O	64
31	GND	-DB08	65
32	GND	-DB09	66
33	GND	-DB10	67
34	GND	-DB11	68

* Terminating resistor power

Figure 1.6 Single-ended connector pin assignment (16-bit SCSI)

Pin No.	Signal	Signal	Pin No.
01	+DB(12)	-DB(12)	35
02	+DB(13)	-DB(13)	36
03	+DB(14)	-DB(14)	37
04	+DB(15)	-DB(15)	38
05	+DB(P1)	-DB(P1)	39
06	+DB(0)	-DB(0)	40
07	+DB(1)	-DB(1)	41
08	+DB(2)	-DB(2)	42
09	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+P_CRCA	-P_CRCA	48
15	GROUND	GROUND	49
16	DIFFSENS	GROUND	50
17	TERMPWR *	TERMPWR *	51
18	TERMPWR *	TERMPWR *	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

* Terminating resistor power

Figure 1.7 Low-Voltage-Differential connector pin assignment (16-bit SCSI)

(2) Interface connector of SCA-2 type 16-bit SCSI

The 16-bit, SCA-2 type SCSI bus connectors of the IDD are 80-pin, unshielded connectors, each having two rows of 40 parallel pins (separated 1.27 mm or 0.05" from each other) (see Figure 1.8).

Figure 1.9 shows the pin assignment of 16-bit, SCA-2 type single-ended SCSI interface connector.

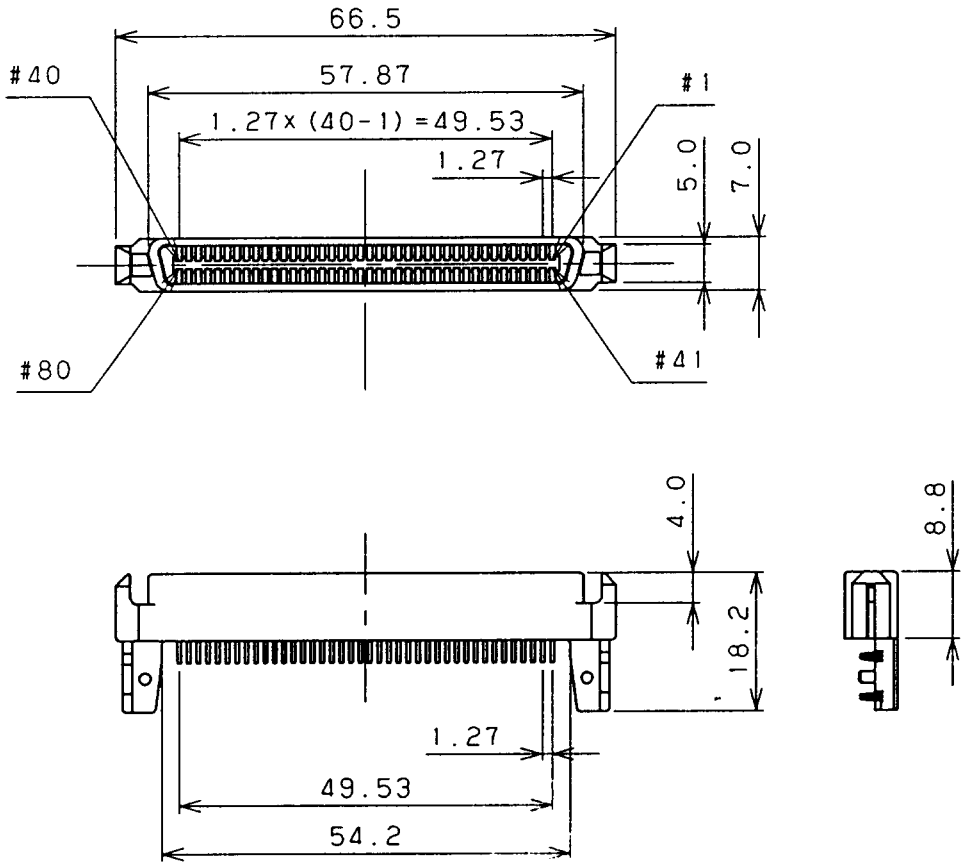


Figure 1.8 SCA-2 type, 16-bit SCSI interface connector (IDD side)

Pin No.	Signal	Signal	Pin No.
01	+12V (CHARGE)	12V RETURN (GND)	41
02	+12V	12V RETURN (GND)	42
03	+12V	12V RETURN (GND)	43
04	+12V	MATED1	44
05	reserved (N.C.)	reserved (N.C.)	45
06	reserved (N.C.)	GND	46
07	-DB11	GND	47
08	-DB10	GND	48
09	-DB09	GND	49
10	-DB08	GND	50
11	-I/O	GND	51
12	-REQ	GND	52
13	-C/D	GND	53
14	-SEL	GND	54
15	-MSG	GND	55
16	-RST	GND	56
17	-ACK	GND	57
18	-BSY	GND	58
19	-ATN	GND	59
20	-P_CRCA	GND	60
21	-DB07	GND	61
22	-DB06	GND	62
23	-DB05	GND	63
24	-DB04	GND	64
25	-DB03	GND	65
26	-DB02	GND	66
27	-DB01	GND	67
28	-DB00	GND	68
29	-DBP1	GND	69
30	-DB15	GND	70
31	-DB14	GND	71
32	-DB13	GND	72
33	-DB12	GND	73
34	5V	5V RETURN (MATED2)	74
35	5V	5V RETURN (GND)	75
36	5V (CHARGE)	5V RETURN (GND)	76
37	Reserved	-LED	77
38	RMT_START	DLYD_START	78
39	SCSI ID0	SCSI ID1	79
40	SCSI ID2	SCSI ID3	80

Note:

Signal in parentheses indicates for SCA-2 type.

Figure 1.9 SCA-2 Type, single-ended 16-bit SCSI connector signal assignment

Pin No.	Signal	Signal	Pin No.
01	+12V (CHARGE)	12V RETURN (GND)	41
02	+12V	12V RETURN (GND)	42
03	+12V	12V RETURN (GND)	43
04	+12V	MATED1	44
05	reserved(N.C.)	reserved(N.C.)	45
06	reserved(N.C.)	DIFFSENS	46
07	-DB(11)	+DB(11)	47
08	-DB(10)	+DB(10)	48
09	-DB(9)	+DB(9)	49
10	-DB(8)	+DB(8)	50
11	-I/O	+I/O	51
12	-REQ	+REQ	52
13	-C/D	+C/D	53
14	-SEL	+SEL	54
15	-MSG	+MSG	55
16	-RST	+RST	56
17	-ACK	+ACK	57
18	-BSY	+BSY	58
19	-ATN	+ATN	59
20	-P_CRCA	+P_CRCA	60
21	-DB(7)	+DB(7)	61
22	-DB(6)	+DB(6)	62
23	-DB(5)	+DB(5)	63
24	-DB(4)	+DB(4)	64
25	-DB(3)	+DB(3)	65
26	-DB(2)	+DB(2)	66
27	-DB(1)	+DB(1)	67
28	-DB(0)	+DB(0)	68
29	-DB(P1)	+DB(P1)	69
30	-DB(15)	+DB(15)	70
31	-DB(14)	+DB(14)	71
32	-DB(13)	+DB(13)	72
33	-DB(12)	+DB(12)	73
34	+5V	5V RETURN (MATED2)	74
35	+5V	5V RETURN (GND)	75
36	+5V (CHARGE)	5V RETURN (GND)	76
37	Reserved	-LED	77
38	RMT_START	DLYD_START	78
39	SCSI ID0	SCSI ID1	79
40	SCSI ID2	SCSI ID3	80

Figure 1.10 SCA Type, Low-Voltage-Differential connector signal assignment

1.3.2 Interface cable

Use the twisted-pair interface cables satisfying the requirements of Tables 1.4 ,1.5.

Table 1.4 SE and LVD Transmission line impedance of cable at maximum indicated data transfer rate

Description	Local SE transmission line impedance		Local differential transmission line impedance	
	Minimum	Maximum	Minimum	Maximum
All	84 Ohms (78 Ohms) (Note)	96 Ohms	110 Ohms	135 Ohms

Note:

If SCSI loads attached to the cable media are separated by more than 1.0 m use the value of 78 Ohms.

Table 1.5 Attenuation Requiaments for SCSI cable media

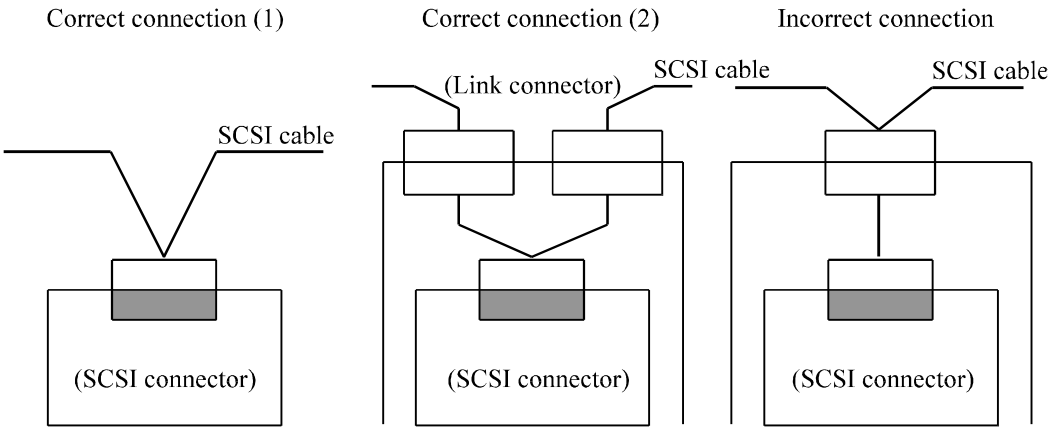
Distance between SCSI bus terminators (meters)	Distances are consistent with these minimum size conductors when used with high quality dielectrics	Notes
0 to 9	0.0324 mm^2 (32 AWG) solid/ 0.05092 mm^2 (30 AWG) stranded	multiple loads allowed
0 to 12	0.05092 mm^2 (30 AWG) solid/ 0.08042 mm^2 (28 AWG) stranded	multiple loads allowed
>12 to 25	0.05092 mm^2 (30 AWG) solid/ 0.08042 mm^2 (28 AWG) stranded	point to point only

A twisted-pair cable must consist of pin n and pin n+1 (where "n" is an odd number) of the interface connector. Use the SCSI bus cables having the same impedance characteristics to minimize the signal reflection but keep the highest possible transmission characteristics.

If SCSI devices are connected to the terminals other than the interface cable ends, use the cable branch at the SCSI connectors. No more SCSI cable can be connected to the last SCSI device (which is connected to the SCSI bus) except when it is terminated with the terminator (see Figure 1.11).

The interface cable must have the stub length less than 0.1 meter for the single-ended SCSI cable. Separate the stabs at least 0.3 meter from each other. (Keep the stab at least 30 cm away from a SCSI device.)

(a) Connection to a middle point of the cable



(b) Connection to the end of the cable.

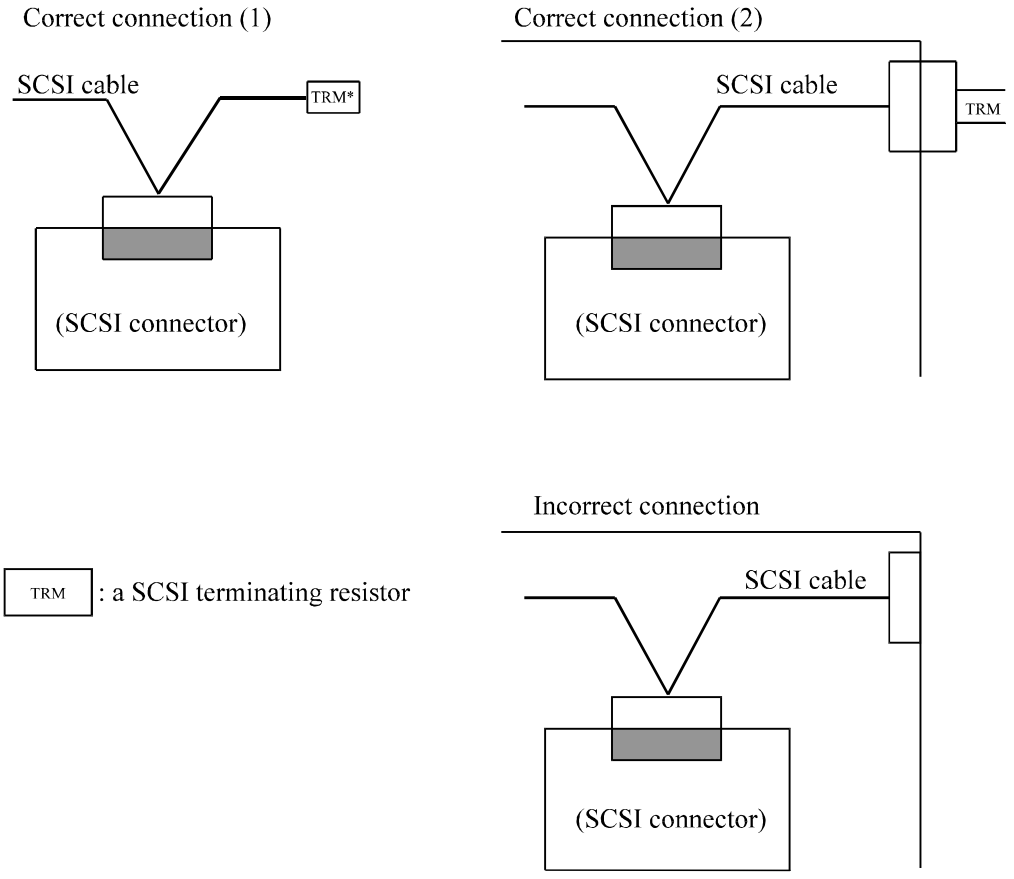


Figure 1.11 Connection of interface cable

1.4 Electrical Requirements

1.4.1 Single-Ended type

(1) Termination circuit

All signals except for RESERVE, GND, or TERMPWR should be terminated at both ends of the bus. Each signal should be terminated by one of the following methods. Figures 1.12 and 1.13 show the termination circuit.

a) Each signal must connect to the TERMPWR signal through 220 Ω (within ±5%) resistor, and connect to ground through 330 Ω (within ±5%) resistor.

b) The termination circuit of each signal shall satisfy the following conditions.

1) The terminators should be powered by the TERMPWR line. The circuit may receive additional power from other sources but not require such additional power for proper operation;

2) Each terminator should source current to the signal line whenever its terminal voltage is below 2.5 VDC and this current should not exceed 22.4 mA for any line voltage at or above 0.5 VDC and 25.4 mA for any line voltage between 0.5 VDC and 0.2 VDC even when all other signal lines are driven at 4.0 VDC;

3) The voltage on all released signal lines should be at least 2.5 VDC;

4) These conditions should be met with any conforming configuration of TARGs and INITs as long as at least one SCSI device is supplying TERMPWR;

5) The terminator at each end of the SCSI bus should add a maximum of 25 pF capacitance to each signal;

6) The terminator may not source current to the signal line whenever its terminal voltage is above 3.24 VDC except terminators may source current when the voltage is above 3.24 VDC in applications where the bus is less than 0.3 m;

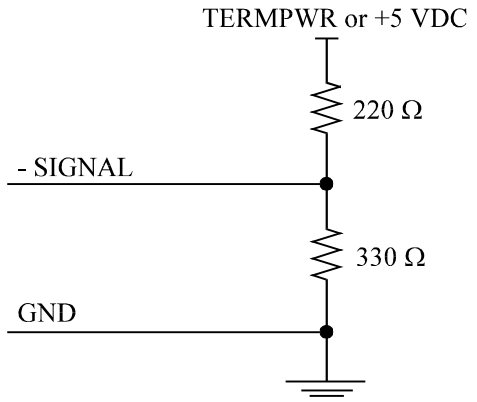
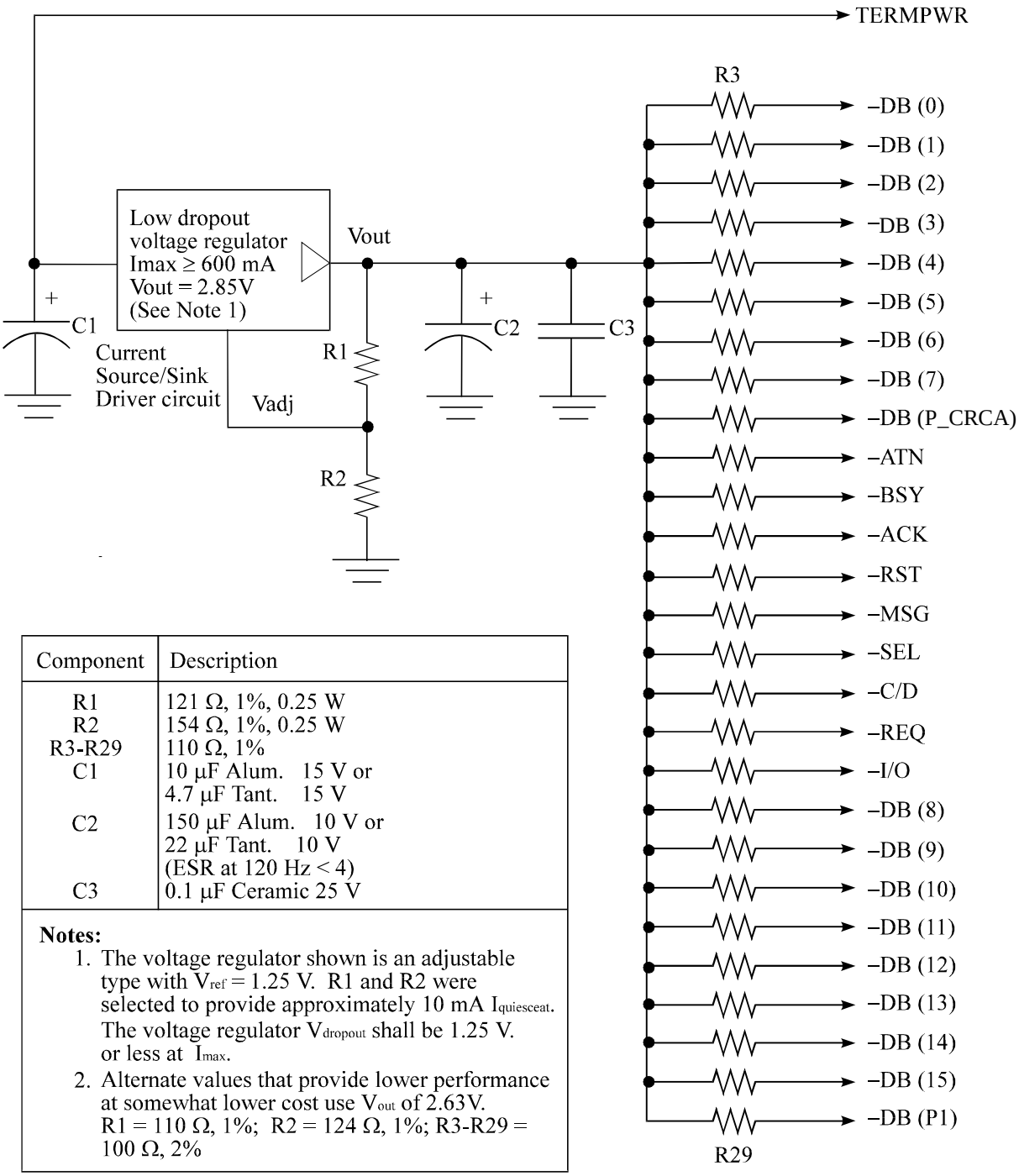


Figure 1.12 Single-Ended SCSI termination circuit-1

The IDD uses the terminator circuit satisfying conditions (b) above. The INIT terminator circuit is also recommended to meet conditions (b) above.



Component	Description
R1	121 Ω, 1%, 0.25 W
R2	154 Ω, 1%, 0.25 W
R3-R29	110 Ω, 1%
C1	10 µF Alum. 15 V or 4.7 µF Tant. 15 V
C2	150 µF Alum. 10 V or 22 µF Tant. 10 V (ESR at 120 Hz < 4)
C3	0.1 µF Ceramic 25 V

Notes:

1. The voltage regulator shown is an adjustable type with V_{ref} = 1.25 V. R1 and R2 were selected to provide approximately 10 mA $I_{quiesceat}$. The voltage regulator $V_{dropout}$ shall be 1.25 V. or less at I_{max}.
2. Alternate values that provide lower performance at somewhat lower cost use V_{out} of 2.63V. R1 = 110 Ω, 1%; R2 = 124 Ω, 1%; R3-R29 = 100 Ω, 2%

Figure 1.13 Single-Ended SCSI termination circuit-2

(2) Driver and receiver

For the interface signal driver, an open-collector or tri-state buffer that satisfies the following output characteristics is used. All signals are negative logic (true = "L").

The receiver and non-driver of the SCSI device under the power-on state should satisfy the following input characteristics on each signal.

Table 1.6 Output characteristic

Driver Type	Value	Min	Max	Notes
Passive Negation	V_{OL}	0.0	0.5	@I_{OL}=48mA
	V_{OH}	2.5	5.25	
Active Negation	V_{OL}	0.0	0.5	@I_{OL}=48mA
	V_{OH}	2.5	3.7	

Table 1.7 Input characteristic

Maximum transfer mode		Min	Max	Notes
Fast-5	V_{IL} [VDC]	-	0.8	
	V_{IH} [VDC]	2.0	-	
	I_{IL} [mA]	-0.4	0.0	@$V_{I=}$ 0.5VDC
	I_{IH} [mA]	0.0	0.1	@$V_{I=}$ 2.7VDC
	Minimum input hysteresis [VDC]	0.2	-	
Fast-10	V_{IL} [VDC]	-	0.8	
	V_{IH} [VDC]	2.0	-	@$V_{I=}$ 0.5VDC
	I_{IL} [μA]	-20	20	@$V_{I=}$ 2.7VDC
	I_{IH} [μA]	-20	20	
	Minimum input hysteresis [VDC]	0.3	-	
Fast-20	V_{IL} [VDC]	-	1.0	
	V_{IH} [VDC]	1.9	-	
	I_{IL} [μA]	-20	20	@$V_{I=}$ 0.5VDC
	I_{IH} [μA]	-20	20	@$V_{I=}$ 2.7VDC
	Minimum input hysteresis [VDC]	0.3	-	

Note:

The SCSI device under the power-off state should satisfy the characteristics of I_{IL} and I_{IH}.

[Recommended circuit example]
Driver:MB463 (Fujitsu) or SN7438 (TI) (Open-collector NAND gate)
Receiver:SN74LS240 or SN74LS19 (TI) (Shumitt trigger input inverter)

1.4.2 Low-Voltage Differential type

(1) Termination circuit

All signals except for GROUND and TERMPWR should be terminated at both ends of the bus. Each signal should be terminated. Figure 1.14 shows the termination circuit.

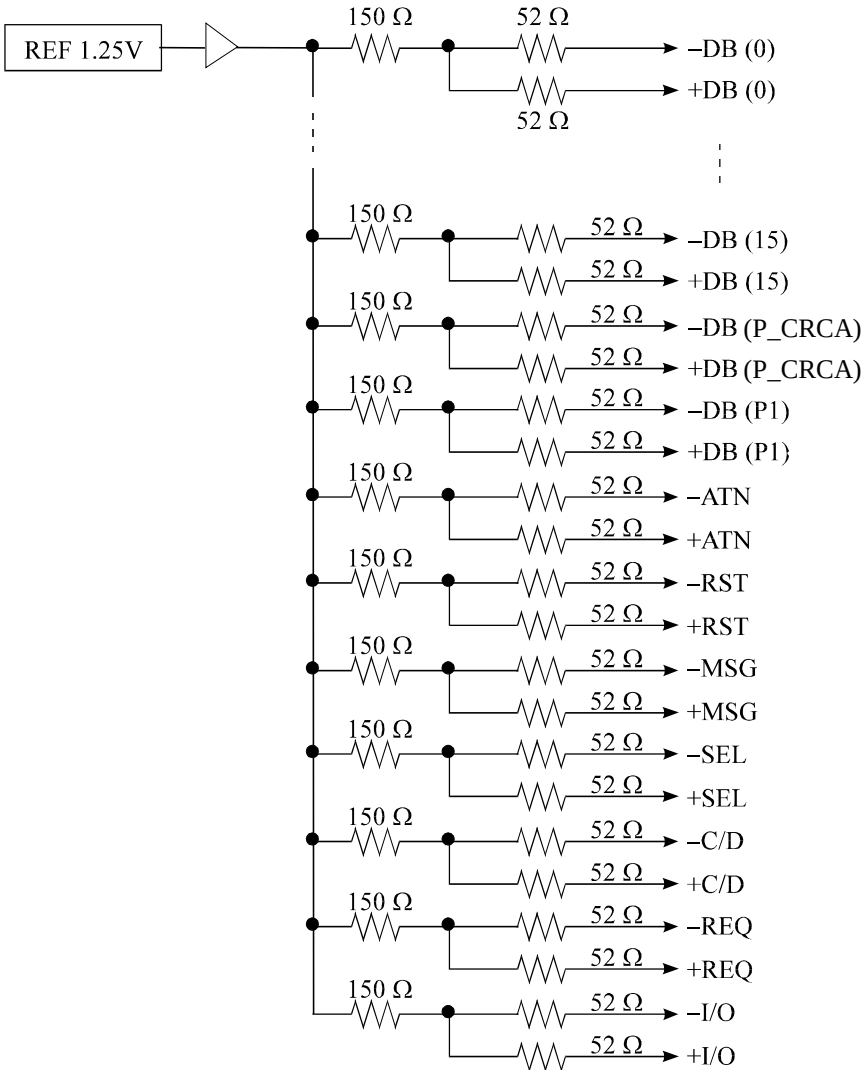


Figure 1.14 LVD SCSI termination circuit

(2) DIFFSENS

a) DIFFSENS driver

The LVD DIFFSENS driver sets a voltage level on the DIFFSENS line that uniquely defines a LVD transmission mode. LVD terminators and multimode terminators shall provide a LVD DIFFSENS driver according to the specifications in Table 1.8.

Table 1.8 LVD DIFFSENS driver specifications

Value	Max.	Nominal	Min	Notes
V_O [V] when I_O=0 (shorted to ground) to 5mA	1.4	1.3	1.2	
I_{OS} [mA]	15	5	-	With TERMPWR at operational levels and V_O=0.
|Input current DC|(μA)	10	-	-	With terminator disabled.
Input sink current D.C. (μA) at V_O=2.75V	200	-	20	Required to prevent the line from floating and to ensure the HVD DIFFSENS driver dominate the LVD

b) DIFFSENS receiver

LVD SCSI devices shall incorporate a LVD DIFFSENS receiver that detects the voltage level on the DIFFSENS line for purposes of informing the device of the transmission mode being used by the bus. The LVD DIFFSENS receiver shall be capable of detecting SE and LVD SCSI devices. Table 1.9 define the receiver input levels for each of the two modes.

Table 1.9 DIFFSENS receiver operating requirements

V_{IN} range	Sensed differential drive type
-0.35 ~ +0.5V	SE
+0.7 ~ +1.9V	LVD

The input resistance requirement is for purposes of providing ground reference if no DIFFSENS drivers are connected to the bus and to ensure that the DIFFSENS receivers do not load the DIFFSENS drivers excessively and to ensure that SE mode is detected.

Devices shall not allow the signal drivers to leave the high impedance state during initial power on until both of the following conditions are satisfied:

a) The device is capable of logical operation for at least 100 ms, and

Notes:

The 100 ms delay allows time for the DIFFSENS pin to connect after the initial power connection (in the case of insertion of a device into an active system), or allows time for the power distribution system to settle.

b) The DIFFSENS mode detected has remained stable for an additional 100 ms after a) is achieved.

A device shall not change its present signal driver or receiver mode based on the DIFFSENS voltage level unless a new mode is sensed continuously for at least 100 ms.

(3) MATED Signals

If MATED 1 and MATED 2 signals are not mated then one or more short pins are not mated. If MATED 1 and MATED 2 signals are mated then the mated condition of the short pins is indeterminate. The MATED 1 and MATED 2 signals may indicate to the SCSI device that the SCSI device is seated in an SCA-2 connector and it may begin power on processing. The signal requirements are indicated below, but may be met by the circuit.

a) MATED 2/Drive Side

The signal is attached to signal ground on the SCSI device side.

b) MATED 2/Backplane Side

The signal is attached either directly or through optional logic in such a manner that the MATED 1 signal is held to a ground level when the MATED 2 connection is completed. The SCSI device shall sink no more than 100 mA to ground through the MATED 2 pin if optional logic is used.

c) MATED 1/Drive Side

The MATED 1 signal shall be sensed by the SCSI device. When the MATED 1 connection is determined to be at a ground level, the SCSI device may assume that the SCSI device has been partially mated. Assuming the mating process continues uninterrupted until competition, including sensing of the SCSI ID Selection signals and the motor start controls, then normal power on procedures may begin 250 msec after the MATED 1 signal is observed to transition to the ground level. When the MATED 1 connection is determined to be at the open level, the SCSI device is not mated. The MATED 1 signal is tied up to a TTL positive level when the SCSI device is not installed. If the SCSI device is mated and operating, it may optionally detect the open level of MATED 1 as an indication that the SCSI device is partially unmated and may be about to be removed. If the SCSI device supports detection of the open level of MATED 1 to prepare itself for power removal or for physical removal from the enclosure, the detection shall occur within 1 second from the time that the Mated 1 open level occurs at the SCSI device.

(4) MATED 1/Backplane Side

The signal shall be held to a ground level when the MATED 2 connection is completed. The MATED 1 signal shall be held to the open level when the MATED 2 connection is not completed.

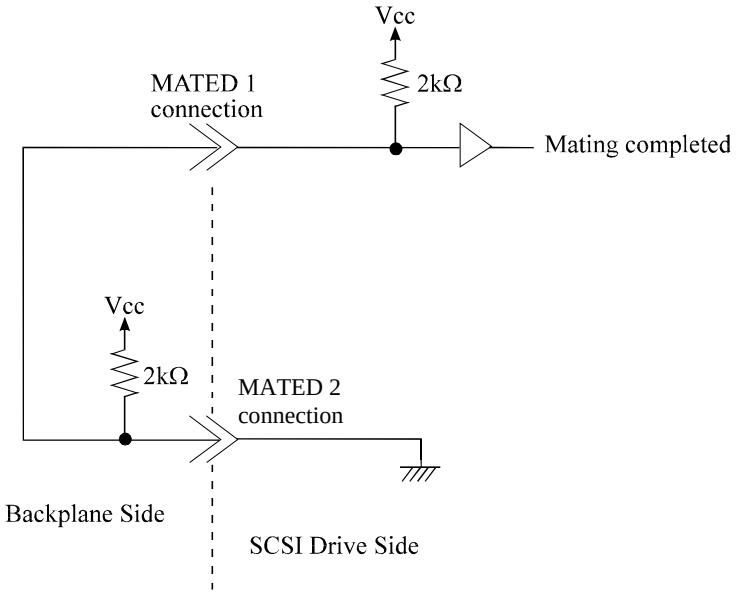


Figure 1.15 Circuit for mated indications

1.4.3 Internal terminal resistor and power supply for terminating resistor

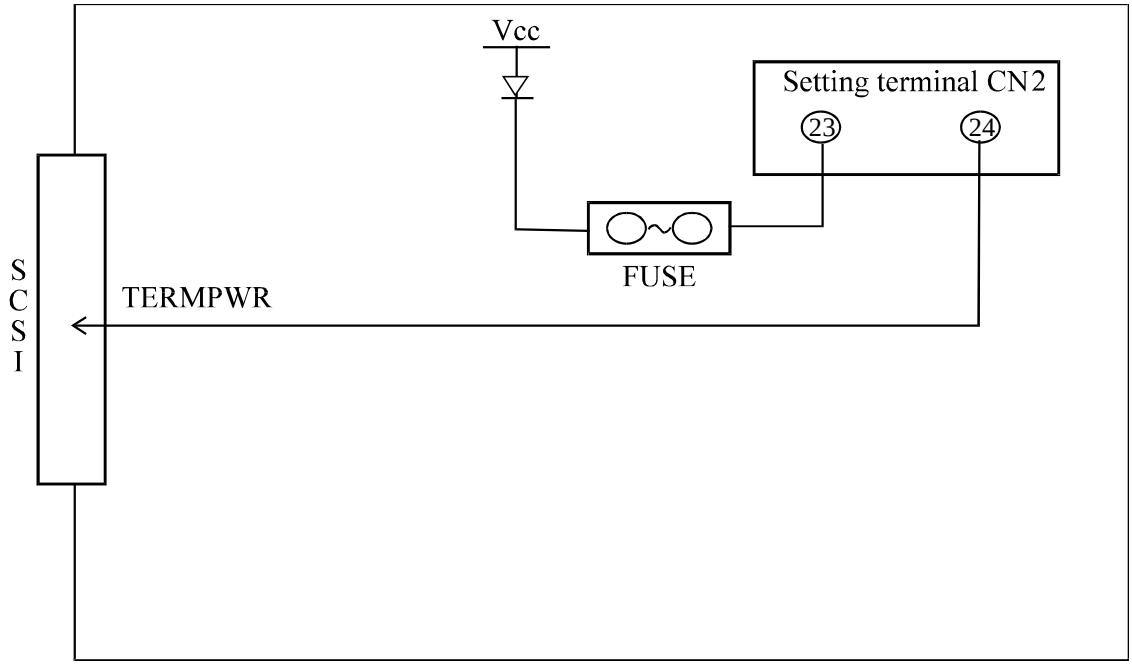
The TERMPWR signal of the interface connector supplies the power to the terminating resistor circuit connected to both ends of the cable. To attach a terminating resistor to an external SCSI device or to cut the power of SCSI device having a terminator, the terminator power must be supplied to the TERMPWR line from any of SCSI devices of the bus. The SCSI device (such as a host adapter) which always operates as the INIT should supply the power. The terminating resistor power shall be supplied to the TERMPWR line through a diode to prevent a reverse current.

Table 1.10 lists the requirements for terminating the resistor power supply (Vterm).

Table 1.10 Requirements for terminating resistor power supply

Terminator Power Characteristics	Terminator Type			
	SE (P Cable)		LVD	SE and LVD type (Multimode)
	0.2V dropout regulator			
I_{min}(A)@V_{min}	0.6	0.6	0.5	0.65
V_{min}(V)@I_{min}	2.7	4.0	3.0	3.0
V_{max}(V)@ all conditions	5.25	5.25	5.25	5.25

Figure 1.16 shows the configuration of a SCSI terminating resistor circuit. The circuit shall be set in either mode (by the CN2 setup pin) depending on the IDD system requirements.



	16-bit SCSI (P-connector) setting terminal CN2 23-24pin
Supply TERMPWR to SCSI Bus	Short
Don’t supply TERMPWR to SCSI Bus	Open

Figure 1.16 16-bit SCSI (not SCA2) terminating resistor circuit

Notes:

All series have no internal terminator circuit. If the terminator circuit is needed, you should add the external circuit on your system.

1.4.4 Usage in 8-bit/16-bit transfer mode

When the IDD is used as 8-bit SCSI device, it is connected terminating resistor circuit to upper 8-bit and parity (DB08 to DB15 and DBP1) or short set up pin (CN2 13-14). When the IDD is used as 16-bit SCSI device, leave the set up pin Jumper setting "8/16" open. Table 1.11 shows the guide. Jumper setting is available only for MP series.

Table 1.11 Setting set up pin, 16-bit (wide)/8-bit (narrow) mode

Transfer mode	Jumper setting "8/16"	DB08 to DB15 and DBP1
8bit (narrow)	Short	Don't care.
	Open	Should be terminated externally.
16bit (wide)	Should be opened	Don't care.

1.4.5 Signal driving conditions

(1) Signal status value

Table 1.12 shows the correspondence between the input interface signal level at the receiving end and its logic state.

Table 1.12 Signal status at receiving end

Logic state	Single-ended type signal state		LVD type signal state
	Asynchronous, Fast-5, Fast-10	Fast-20	
True, "1", or asserted	Low (less than 0.8 VDC)	Low (less than 1.0 VDC)	Low (-3.6 to -0.030 VDC)
False, "0", negated or released	High (more than 2.0 VDC)	High (more than 1.9 VDC)	High (0.030 to 3.6 VDC)

(2) Signal driving method

Two driving methods are available: "OR-tied" type and "non-OR-tied" type as indicated in Table 1.13.

Table 1.13 Signal driving method

Driving method / Signal status	"OR-tied" type	"non-OR-tied" type
False (*1)	No SCSI device drives a signal. The signal becomes false when the terminating resistor circuit is biased.	A particular SCSI device drives the signal false. Otherwise, no SCSI device drives the signal.
True	A SCSI device drives the signal true	

*1 In this manual, the signal is said to be false if one of the following conditions is satisfied.

1. The signal is actually driven by a SCSI device to become false (non-OR-tied type).
2. No SCSI device is driving the signal (OR-tied type or non-OR-tied type).

If the BSY, SEL and RST signals may be driven by two or more SCSI devices simultaneously in the interface operating sequence, they must be driven in the OR-tied method. All signals except for SEL, BSY, RST and DB(P_CRCA, P1) are not driven by multiple SCSI devices simultaneously. However, the DBP signals must be driven false in the ARBITRATION phase. All signals driven in OR-tied and non-OR-tied method can be mixed on the same signal line of SCSI bus except for BSY, SEL and RST signals.

(3) Signal sources

Table 1.14 lists SCSI device types (or signal sources) which can drive signals in each interface operating phase.

Table 1.14 Bus phases and signal sources

	BSY	SEL	I/O, REQ, C/D, MSG	ACK, ATN	DB7-0	DB15-8, DBP1	P_CRCA	RST
BUS FREE	N	N	N	N	N	N	N	A
ARBITRATION	A	W	N	N	ID	ID	ID	A
QAS ARBITRATION	PT	W	N	N	ID	ID	ID	ID
SELECTION	I&T	I	N	I	I	I	I	A
RESELECTION	I&T	T	T	I	T	T	T	A
COMMAND	T	N	T	I	I	N	I	A
ST DATA IN	T	N	T	I	T	T	T	A
ST DATA OUT	T	N	T	I	I	I	I	A
DT DATA IN	T	N	T	I	T	T	T	A
DT DATA OUT	T	N	T	I	I	I	T	A
STATUS	T	N	T	I	T	N	T	A
MESSAGE IN	T	N	T	I	T	N	T	A
MESSAGE OUT	T	N	T	I	I	N	I	A

A: Any SCSI device can drive the signal. Also, two or more SCSI devices may drive the signal simultaneously.

I: Only the INIT SCSI device drives the signal.

I&T: The INIT and TARG SCSI devices drive the signal in the interface operating sequence. INIT, TARG or both can drive this signal according to the interface sequence.

I or T: The INIT or TARG SCSI device (or both devices) may drive the signal depending on the I/O signal status and bus width.

ID: Each SCSI device which is actively arbitrating the bus drives a unique data bit (SCSI ID). The parity bit may be undriven or driven to the true state, but must never be driven to the false state.

N: Not be driven by any SCSI device.

T: Only the TARG SCSI device drives the signal.

W: Only a single SCSI device selected through arbitration drives the signal.

1.5 Timing Rule

1.5.1 Timing value

Table 1.15, 16, 17 give the timing required for operations on the SCSI bus.

Table 1.15 SCSI bus control timing values

	Timing description	Type	Timing values
1	Arbitration delay	Min	2.4 μs
2	Bus clear delay	Max	800 ns
3	Bus free delay	Min	800 ns
4	Bus set delay	Max	1.6 μs
5	Bus settle delay	Min	400 ns
6	Cable skew (1)	Max	4 ns
7	Data release delay	Max	400 ns
8	DIFFSENS voltage filter time	Min	100 ms
9	Physical disconnection delay	Min	200 μs
10	Power on to selection (2)	Max	10 s
11	QAS arbitration delay	Min	1000 ns
12	QAS assertion delay	Max	200 ns
13	QAS release delay	Max	200 ns
14	QAS non-DATA phase REQ(ACK) peiod	Min	50 ns
15	Reset delay	Min	200 ns
16	Reset hold time	Min	25 μs

Note: (1) Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew. (2) This is a recommended time. It is not mandatory.

Table 1.16 SCSI bus data & information phase ST timing values

	Timing description	Type	Timing values [ns] (5)				
			Async	Fast-5	Fast-10	Fast-20	Fast-40
1	ATN Transmit Setup Time	min.	90	33	33	21.5	19.25
2	ATN Receive Setup Time	min.	45	17	17	8.5	6.75
3	Cable Skew (3)	max.	4	4	4	3	2.5
4	Receive Assertion Period (4)	min.	N/A	70	22	11	6.5
5	Receive Hold Time (4)	min.	N/A	25	25	11.5	4.75
6	Receive Negation Period (4)	min.	N/A	70	22	11	6.5
7	Receive Setup Time (4)	min.	N/A	15	15	6.5	4.75
8	Receive REQ (ACK) Period Tolerance	min.	N/A	1.1	1.1	1.1	1.1
9	Signal Timing Skew	max.	8	8	8	5	4.5
10	REQ (ACK) Period	min.	N/A	200	100	50	25
11	Transmit Assertion Period (4)	min.	N/A	80	30	15	8
12	Transmit Hold Time (4)	min.	N/A	53	33	16.5	9.25
13	Transmit Negation Period (4)	min.	N/A	80	30	15	8
14	Transmit Setup Time (4)	min.	N/A	23	23	11.5	9.25
15	Transmit REQ (ACK) Period Tolerance	max.	N/A	1	1	1	1

Note: (3) Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew. (4) See Fig.1-17,18,19 for measurement points for the timing specifications. (5) SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

Table 1.17 Miscellaneous SCSI bus data & information phase DT timing values

	Timing description	Type	Timing values [ns] (7)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
1	Cable skew(6)	Max	4	3	2.5	2.5	2.5
2	REQ(ACK) period	Nominal	200	100	50	25	12.5
3	Residual Skew Error(8)	Max	N/A	N/A	N/A	N/A	±0.15
4	De-skewed data valid window(9)	Min	N/A	N/A	N/A	N/A	±2.1
5	Skew correction range(9)	Min	N/A	N/A	N/A	N/A	±3.65(10)
6	Signal timing skew	Max	26.8	13.4	6.7	3.35	4.85
7	Strobe Offset Tolerance	Max	N/A	N/A	N/A	N/A	±0.125
Fast-160 SCSI devices shall not change timing parameters between training or reset events.							

Note: (6)Cable skew is measured at each SCSI device connection within the same bus segment with the transmitted skew subtracted from the received skew. (7) SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated. (8) Calculated assuming timing budget shown in table 46. (9) Measured at the receiver terminal using clean input signals with 500 mV peak amplitude and 1 ns rise and fall time between 20 % and 80 % of the signal. (10) Relative to the REQ(ACK) clocking signal.

Table 1.18 SCSI bus data & information phase DT timing values

	Timing description	Type	Timing values [ns] (12)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
1	ATN transmit setup time	Min	48.4	29.2	19.6	14.8	14
2	Flow control transmit hold time	Min	38.4	19.2	9.6	4.8	1.4
3	Flow control transmit setup time	Min	48.4	29.2	19.6	14.8	1.4
4	pCRC transmit hold time	Min	38.4	19.2	9.6	4.8	N/A
5	pCRC transmit setup time	Min	48.4	29.2	19.6	14.8	N/A
6	Transmit assertion period (11)	Min	92	46	23	11.5	5.69
7	Transmit hold time (11)	Min	38.4	19.2	9.6	4.8	4.77
8	Transmit ISI Compensation	Max	N/A	N/A	N/A	N/A	1.0
9	Transmit negation period (11)	Min	92	46	23	11.5	5.69
10	Transmit REQ(ACK) period tolerance	Max	0.6	0.6	0.6	0.6	0.06
11	Transmit REQ assertion period with P_CRCA transitioning	Min	97.5	54	35.5	24	N/A
12	Transmit REQ negation period with P_CRCA transitioning	Min	97.5	54	35.5	24	N/A
13	Transmit setup time (11)	Min	38.4	19.2	9.6	4.8	-1.48
14	Transmitter skew	Max	N/A	N/A	N/A	N/A	±0.75
15	Transmitter time asymmetry	Max	N/A	N/A	N/A	N/A	±0.25
Fast-160 SCSI devices shall not change timing parameters between training or reset events.							

Note: (6) Cable Skew is measured at each device connection with the transmitted skew subtracted from the received skew. (7) See Fig.1-20 for measurement points for the timing specifications. (8) SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

Table 1.19 Receive SCSI bus data & information phase DT timing values

	Timing description	Type	Timing values [ns] (15)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
1	ATN receive setup time	Min	13.6	7.8	4.9	3.45	3
2	Flow control receive hold time	Min	11.6	5.8	2.9	1.45	3
3	Flow control receive setup time	Min	18.6	12.8	9.9	8.45	3
4	PCRC receive hold time	Min	11.6	5.8	2.9	1.45	N/A
5	PCRC receive setup time	Min	18.6	12.8	9.9	8.45	N/A
6	Receive assertion period (14)	Min	80	40	20	8.5	4.74
7	Receive hold time (14)	Min	11.6	5.8	2.9	1.45	-0.08
8	Receive negation period (14)	Min	80	40	20	8.5	4.74
9	Receive setup time (14)	Min	11.6	5.8	2.9	1.45	-6.33
10	Receive REQ(ACK) period tolerance	Min	0.7	0.7	0.7	0.7	0.06
11	Receive REQ assertion period with P_CRCA transitioning	Min	85.5	48	32.5	21	N/A
12	Receive REQ negation period with P_CRCA transitioning	Min	85.5	48	32.5	21	N/A
13	Receive Skew Compensation	Max	N/A	N/A	N/A	N/A	4.4
14	Receive Internal Hold Time	Min	N/A	N/A	N/A	N/A	0.345
15	Receive Internal Setup Time	Min	N/A	N/A	N/A	N/A	0.345
Fast-160 SCSI devices shall not change timing parameters between training or reset events.							

Note: (14) See Fig.1-20,21,22,23,24 for measurement points for the timing specifications. (15) SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

(1) ATN transmit setup time

The minimum time provided by the transmitter between the assertion of the ATN signal and the negation of the ACK signal.

Specified to provide the increased ATN receive setup time, subject to intersymbol interference, cable skew, and other distortions.

(2) ATN receive setup time

The minimum time required at the receiver between the assertion of the ATN signal and the negation of the ACK signal to recognize the assertion of an Attention Condition.

Specified to ease receiver timing requirements.

(3) Arbitration delay

The minimum time a SCSI device shall wait from asserting the BSY signal for arbitration until the DATA BUS is examined to see if arbitration has been won. There is no maximum time.

(4) Bus clear delay

The maximum time that for a SCSI device to release all SCSI signals after:

a) The BUS FREE phase is detected (the BSY and SEL signals are both false for a bus settle delay);
b) The SEL signal is received from another SCSI device during the ARBITRATION phase;
c) The transition of the RST signal to true.

For item a) above, the maximum time for a SCSI device to release all SCSI bus signals is 1200 ns from the BSY and SEL signals first becoming both false. If a SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall release all SCSI bus signals within a bus clear delay minus the excess time.

(5) Bus free delay

The minimum time that a SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of the BSY signal in preparation for entering the ARBITRATION phase.

(6) Bus set delay

The maximum time for a SCSI device to assert the BSY signal and its SCSI ID after it detects a BUS FREE phase for the purpose of entering the ARBITRATION phase.

(7) Bus settle delay

The minimum time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

Provides time for a signal transition to propagate from the driver to the terminator and back to the driver.

(8) Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

(9) Data release delay

The maximum time for an initiator to release the DATA BUS, DB(P_CRCA), DB(P1) signals following the transition of the I/O signal from false to true.

(10) DIFFSENS voltage filter time

The minimum time DIFFSENS voltage shall be sensed continuously within the voltage range of a valid SCSI bus mode.

(11) Physical Disconnection delay

The minimum time that a target shall wait after releasing BSY before participating in an ARBITRATION phase when honoring a DISCONNECT message from the initiator.

(12) Power on to selection

The recommended maximum time from power application until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI-3 Primary Commands Standard.)

(13) Reset delay

The minimum time that the RST signal shall be continuously true before the SCSI device shall initiate a reset.

(14) Reset hold time

The minimum time that the RST signal is asserted. There is no maximum time.

(15) Reset to selection

The recommended maximum time from after a reset condition until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI-3 Primary Commands Standard).

(16) Selection abort time

The maximum time that SCSI device shall take from its most recent detection of being selected or reselected until asserting the BSY signal in response. This time-out is required to ensure that a target or initiator does not assert the BSY signal after a SELECTION or RESELECTION phase has been aborted.

(17) Selection time-out delay

The minimum time that an initiator or target should wait for a assertion of the BSY signal during the SELECTION or RESELECTION phase before starting the time-out procedure. Note that this is only a recommended time period.

(18) System deskew delay

The minimum time that a SCSI device should wait after receiving a SCSI signal to ensure that any signals transmitted at the same time are valid. The system deskew delay shall not be applied to the synchronous data transfers.

(19) Receive assertion period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0.8 V level. For SE fast-20 operation the period is measured at the 1.0 V level. For LVD see figure 1.19 and 1.20 for signal measurement points.

(20) Receive hold time

For ST data transfers the minimum time required at the receiving SCSI device between the assertion of the REQ or ACK signal and the changing of the DB(15-0, P_CRCA, and/or P1) signals while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled.

For DT data transfers the minimum time required at the receiving SCSI device between the transition (i.e. assertion or negation) of the REQ or ACK signals and the changing of the DB(15-0, P_CRCA, and/or P1) signals while using synchronous data transfers.

(21) Receive negation period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2.0 V level. For SE fast-20 operation the period is measured at the 1.9 V level. For LVD see figure 1.19 and figure 1.20 for signal measurement points.

(22) Receive setup time

For ST data transfers the minimum time required at the receiving SCSI device between the changing of the DB(15-0, P_CRCA, and/or P1) signals and the assertion of the REQ or ACK signal while using synchronous data transfers.

For DT data transfers the minimum time required at the receiving SCSI device between the changing of the DB(15-0, P_CRCA, and/or P1) signals and the transition of the REQ or ACK signals while using synchronous data transfers.

(23) Receive REQ(ACK) period tolerance

The minimum tolerance that a SCSI device should allow to be subtracted from the REQ(ACK) period. The tolerance comprises the Transmit REQ(ACK) tolerance plus a measurement error due to noise.

(24) Signal timing skew

The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ or ACK signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101...patterns) and signal distortion skew caused by random data patterns and transmission line reflections. The receiver detection range is the part of the signal between the “may detect” level and the “shall detect” level on either edge.

(25) REQ (ACK) period

The REQ (ACK) period during synchronous data transfers is measured from an assertion edge of the REQ (ACK) signal to the next assertion edge of the signal. In DT DATA phases the nominal transfer period for data is half that of the REQ (ACK) period during synchronous data transfers since data is qualified on both the assertion and negation edges of the REQ (ACK) signal. In ST DATA phases the nominal transfer period for data is equal to the REQ (ACK) period during synchronous data transfers since data is only qualified the assertion edge of the REQ (ACK) signal.

(26) Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

(27) Transmit hold time

For ST data transfers the minimum time provided by the transmitting SCSI device between the assertion of the REQ or ACK signal and the changing of the DB(15-0, P_CRCA, and/or P1) signals while using synchronous data transfers.

For DT data transfers the minimum time provided by the transmitting SCSI device between the transition (i.e. assertion or negation) of the REQ or ACK signals and the changing of the DB(15-0, P_CRCA, and/or P1) signals while using synchronous data transfers.

(28) Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

(29) Transmit setup time

For ST data transfers the minimum time provided by the transmitting SCSI device between the changing of the DB(15-0, P_CRCA, and/or P1) signals and the assertion of the REQ or ACK signal while using synchronous data transfers.

For DT data transfers the minimum time provided by the transmitting SCSI device between the changing of the DB(15-0, P_CRCA, and/or P1) signals and the transition of the REQ or ACK signal while using synchronous data transfers.

(30) Transmit REQ (ACK) period tolerance

The maximum tolerance that a SCSI device may subtract from the negotiated synchronous period.

The tolerance comprises the transmit REQ (ACK) tolerance plus a measurement error due to noise.

(31) pCRC Receive hold time

The minimum time required at the receiver between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled.

(32) pCRC Receive setup time

The minimum time required at the receiver between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled.

Specified to ease receiver timing requirements and ensure that this signal, which is outside CRC protection, is received correctly.

(33) pCRC Transmit hold time

The minimum time provided by the transmitter between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled.

(34) pCRC Transmit setup time

The minimum time provided by the transmitter between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled.

Specified to provide the increased receive setup time, subject to intersymbol interference, cable skew, and other distortions.

(35) Receive REQ assertion period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled.

Specified to ensure that the assertion period is longer than the receive hold time plus the receive setup time.

(36) Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving an REQ signal for the signal to be negated while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled.

Specified to ensure that the negation period is longer than the receive hold time plus the receive setup time.

(37) Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

Specified to provide the increased receive REQ assertion period, subject to loss on the interconnect.

(38) Transmit REQ negation period with P_CRCA transitioning

The minimum time that a target shall negate the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

Specified to provide the increased receive REQ negation period, subject to loss on the interconnect.

(39) QAS arbitration delay

The minimum time a SCSI device with QAS enabled (see 1.6.2.2) shall wait from the detection of the MSG, C/D, and I/O signals being false to start QAS until the DATA BUS is examined to see if QAS has been won (see 1.6.2.2).

(40) QAS assertion delay

The maximum time allowed for a SCSI device to assert certain signals during QAS.

(41) QAS release delay

The maximum time allowed for a SCSI device to release certain signals during QAS.

(42) QAS non-DATA phase REQ(ACK) period

The minimum time a QAS-capable SCSI INIT port shall ensure the REQ and ACK signals are asserted and that data is valid during COMMAND, MESSAGE, and STATUS phases.

(43) Residual skew error

The maximum timing error between the deskewed data and REQ or ACK internal to the receiving SCSI device after skew compensation.

(44) De-skewed data valid window

The minimum difference in time allowed between the rising or falling edge of a "1010..." pattern on the DATA BUS or DB(P1) and its clocking signal on the ACK or REQ signal as measured at their zero-crossing points after skew compensation is applied by the receiver without allowing any error in the received data (see Fig.1-17). The de-skewed data valid window shall be equal to: ± [(data transfer period) - (residual skew error) - (strobe offset tolerance) - (clock jitter) - (receiver amplitude skew) - (chip noise) - (system noise at receiver) - (receiver asymmetry)] / 2.

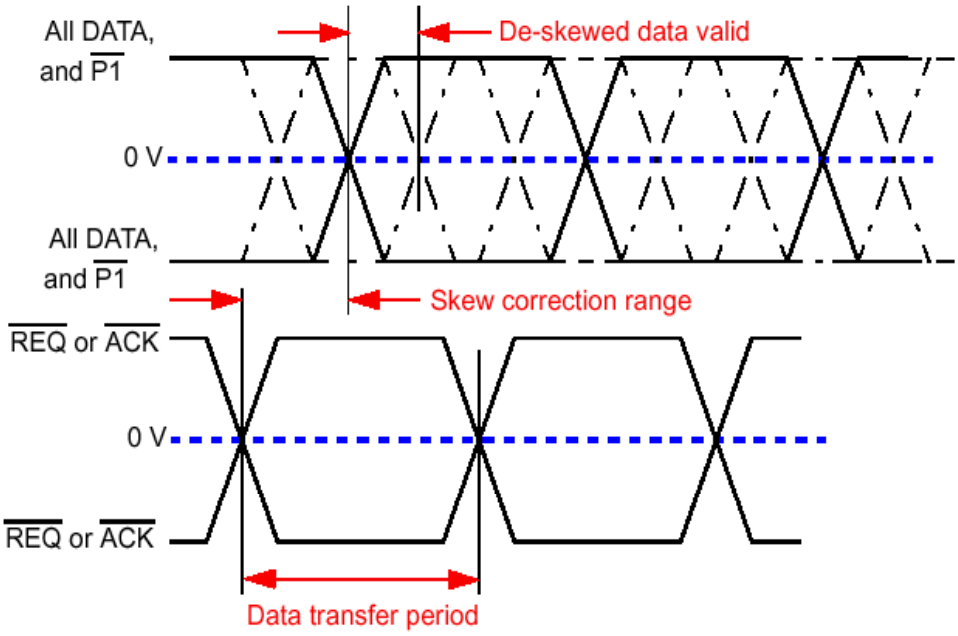


Figure 1.17 Receiver de-skew parameters

(45) Skew correction range

The minimum skew correction capability of the receiver of a signal on the DATA BUS or DB(P1) relative to the ACK or REQ signal as measured at the receiver's connector. The skew correction range shall be equal to ± [(transmitter chip skew) + (cable skew) + (two times trace skew)] relative to the corresponding ACK or REQ clock signal for that transition. Receiver chip skew is not included, as it is internal to the receiver.

(46) Strobe offset tolerance

The time tolerance of centering the compensated REQ or ACK strobe in the transfer period during the training pattern.

(47) Flow control receive hold time

The maximum time required by the SCSI INIT port between the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data stream information unit and the changing of the P_CRCA signal.

(48) Flow control receive setup time

The maximum time required by the SCSI INIT port between the assertion of the P_CRCA signal and the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data stream information unit. Also, the maximum time required by the SCSI INIT port between the negation of the P_CRCA signal and the assertion of the REQ signal corresponding to any valid data transfer of a SPI L_Q information unit.

(49) Flow control transmit hold time

The minimum time provided by the SCSI TARG port between the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data stream information unit and the changing of the P_CRCA signal. Specified to provide the increased P_CRCA receive setup time, subject to intersymbol interference, cable skew, and other distortions.

(50) Flow control transmit setup time

The minimum time provided by the SCSI TARG port between the assertion of the P_CRCA signal and the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data stream information unit. Also, the minimum time provided by the SCSI TARG port between the negation of the P_CRCA signal and the assertion of the REQ signal corresponding to any valid data transfer of a SPI L_Q information unit. Specified to provide the increased P_CRCA receive setup time, subject to intersymbol interference, cable skew, and other distortions.

(51) Receive internal hold time

The minimum time provided for hold time in the receive data detector after allowance for timing errors and timing compensation from all sources measured from the worse case bit (i.e., data or parity) to the compensated offset strobe.

Note:This time may not be observable to other than the SCSI device designer.

(52) Receive internal setup time

The minimum time provided for setup time in the receive data detector after allowance for timing errors and timing compensation from all sources measured from the worse case bit (i.e., data or parity) to the compensated offset strobe.

Note: This time may not be observable to other than the SCSI device designer.

(53) Receive Skew Compensation

The effective reduction in worse case timing skew of data, parity, and strobe signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.

(54) Transmit ISI Compensation

The effective reduction in worse case ISI timing shift provided by the transmitting SCSI device as seen at the receiving SCSI device connector.

(55) Transmitter skew

The maximum difference in time allowed between the rising or falling edge of a "1010..." pattern on the DATA BUS or DB(P1) signal and its clocking signal on the ACK or REQ signal as measured at their zero-crossing points (see Fig.1-18).

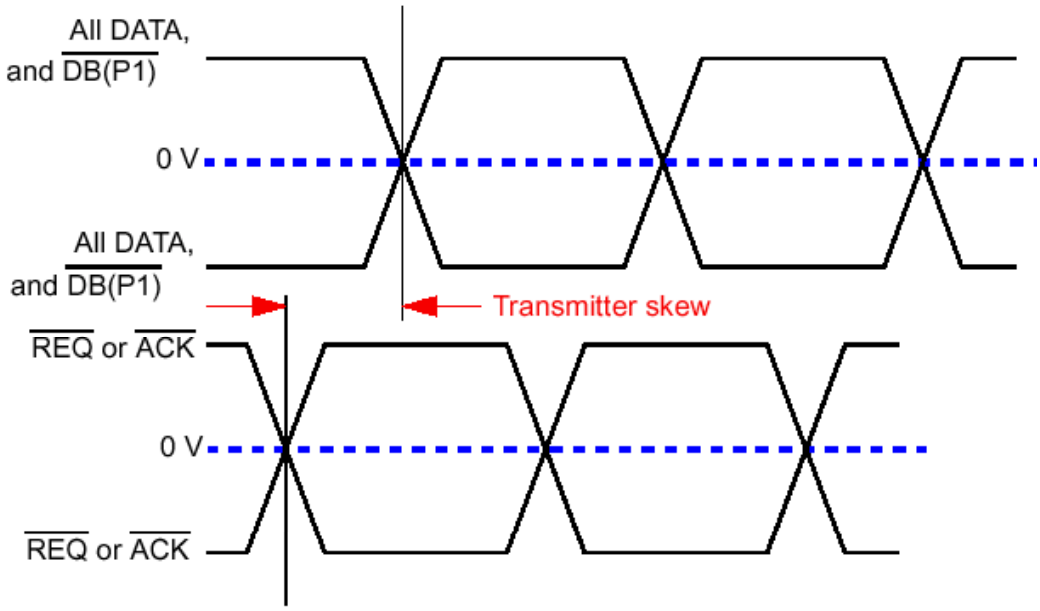


Figure 1.18 Transmitter skew

(56) Transmitter time asymmetry

The maximum time on DATA BUS, DB(P1), ACK, or REQ signal from any transition edge to the subsequent transition edge during a "1010..." pattern, as measured at their zero-crossing points, minus the data transfer period (see Fig.1-19).

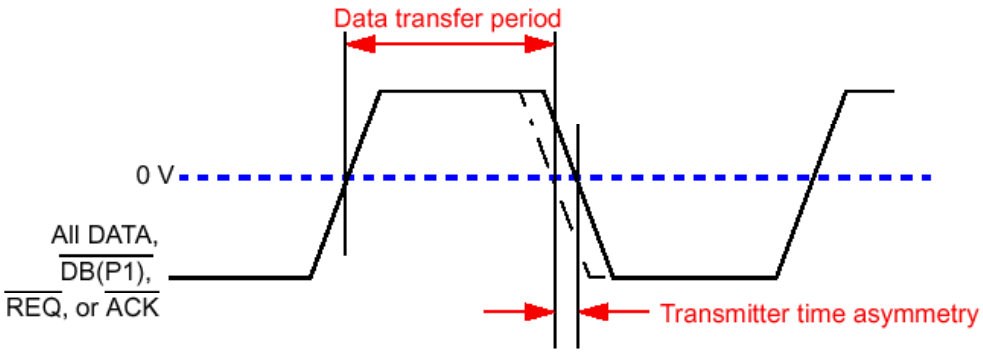


Figure 1.19 Transmitter time asymmetry

1.5.2 Measurement point

(1) SE Fast-5/10

The measurement point of Fast-5/10 is different from that of Fast-20. The Figure 1.20 is the Fast-5/10 measurement point.

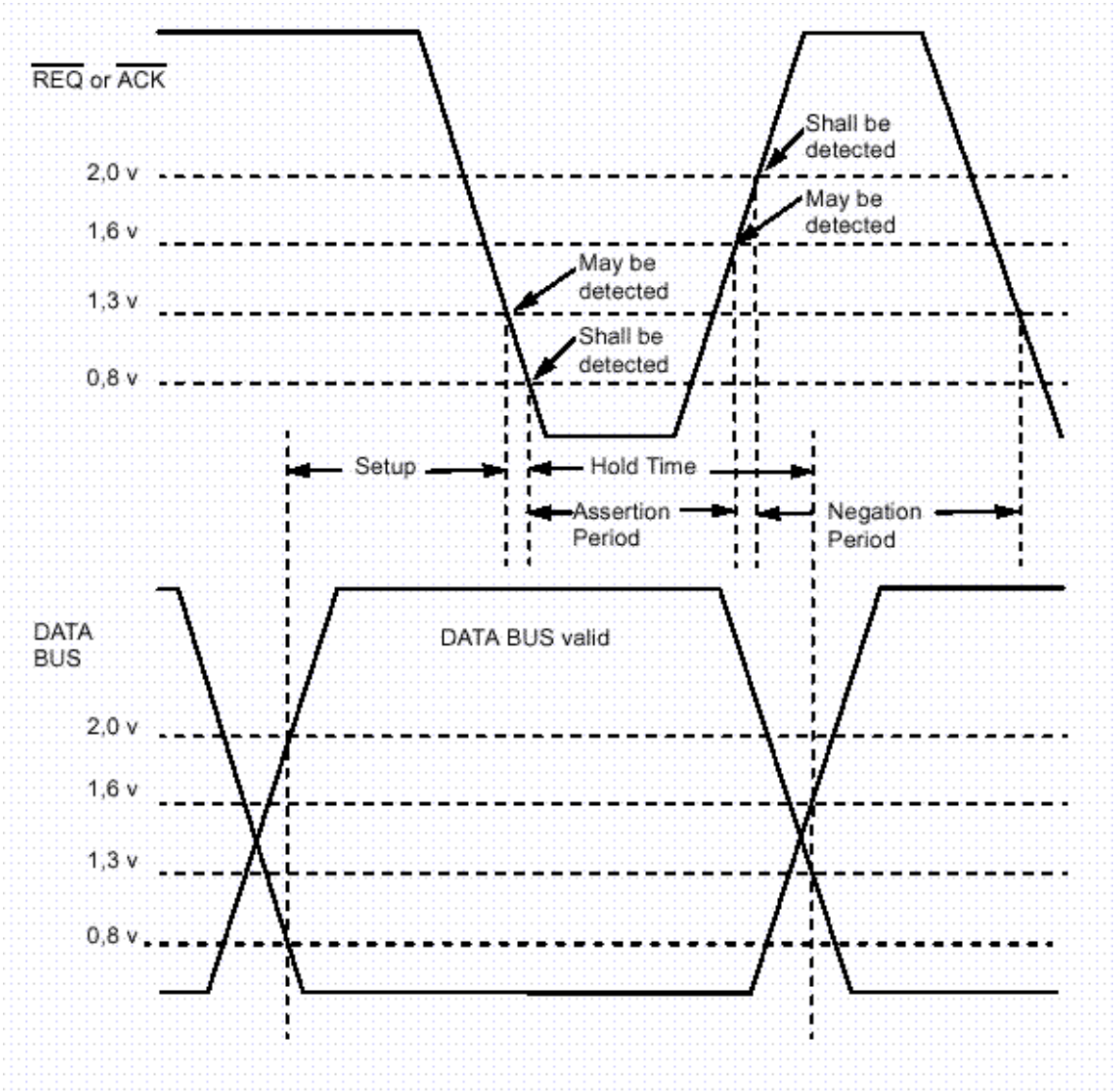


Figure 1.20 Fast-5/10 Measurement Point

(2) SE Fast-20

Figure 1.21 is the Fast-20 measurement point.

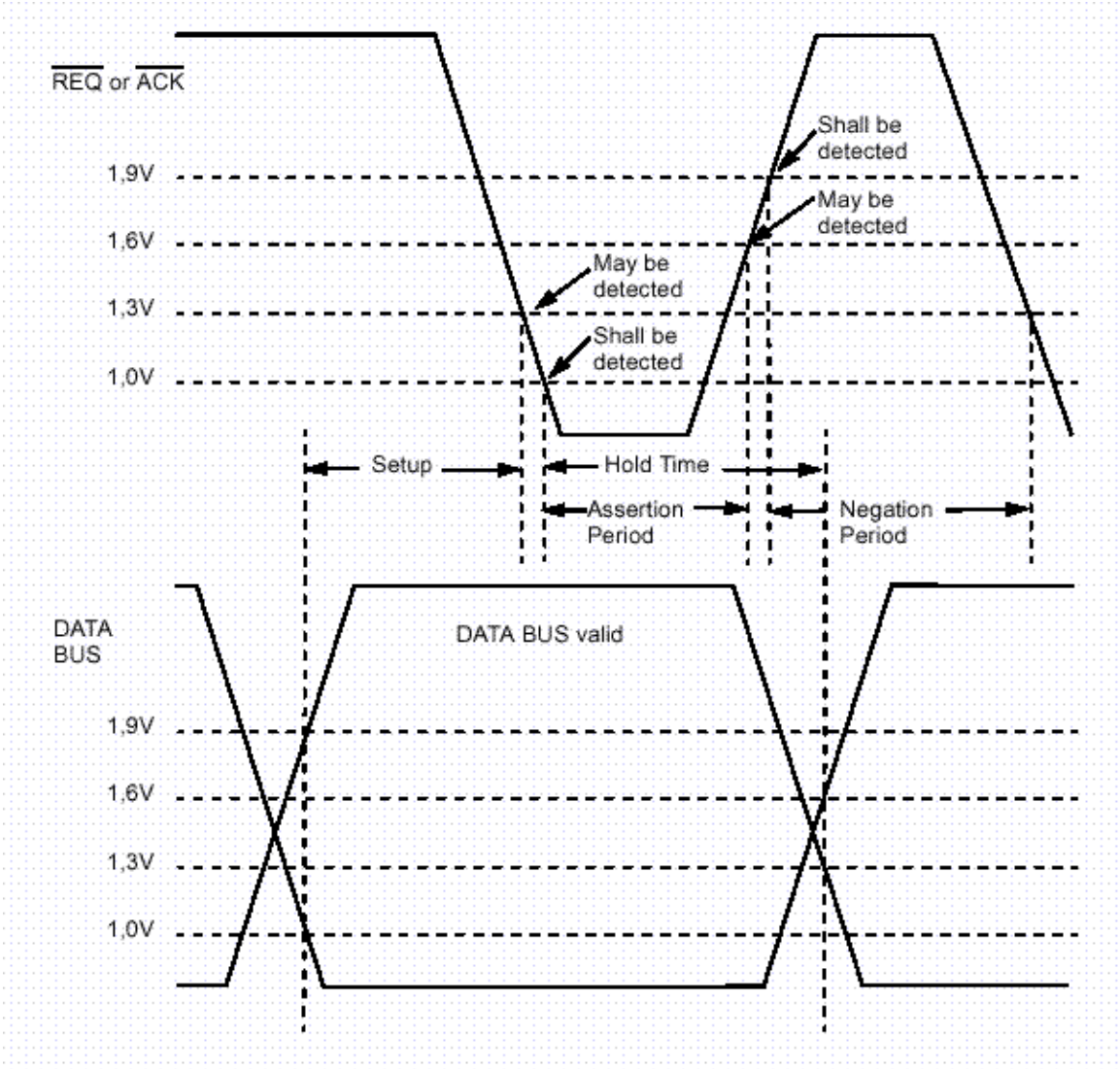


Figure 1.21 Fast-20 Measurement Point

(3) LVD ST Data Transfer

Figure 1.22 is the LVD ST Data Transfer measurement point.

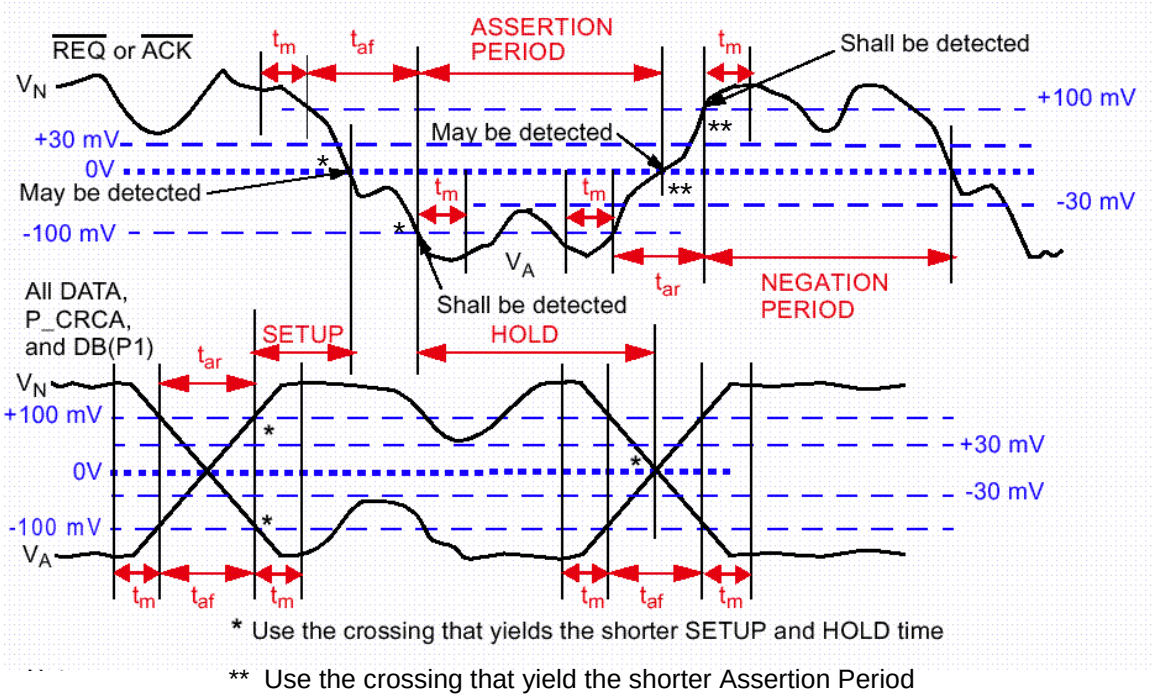


Figure 1.22 LVD ST Data Transfer measurement point

Notes:

1. V_N - negated signal
2. V_A - asserted signal
3. t_m = 1.25ns minimum
4. V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.
5. Differential voltage signals in all cases.
6. t_{af} and t_{ar} shall be less than 3 ns.
7. Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

(4) LVD DT Data Transfer

Figure 1.23 is the LVD DT Data Transfer measurement point.

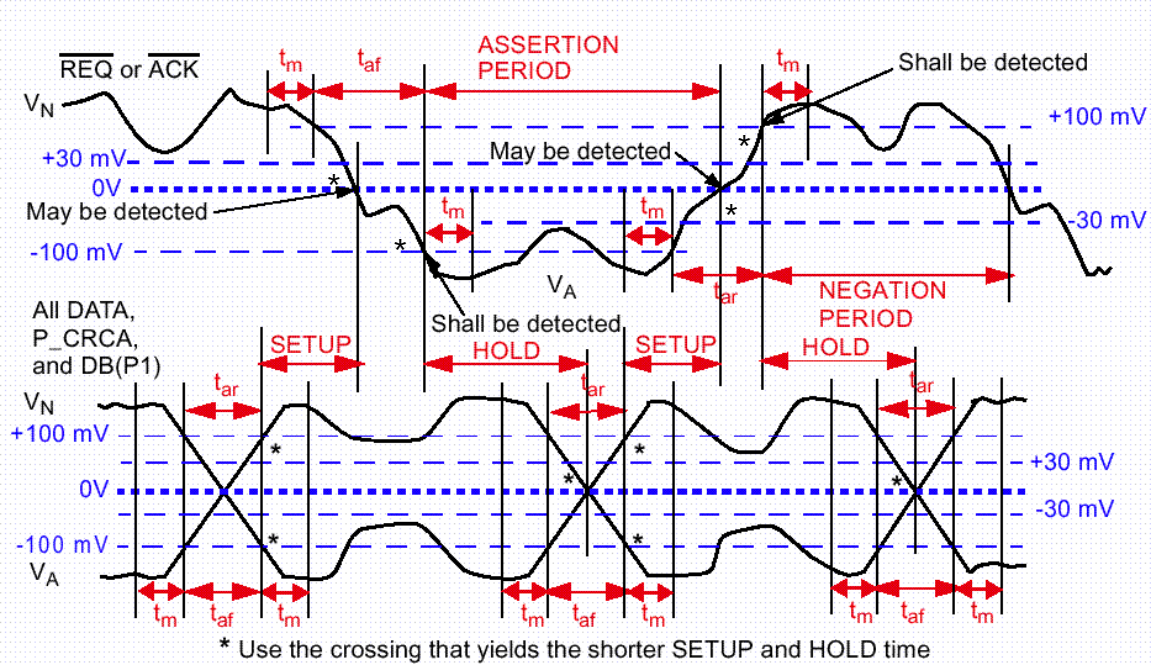


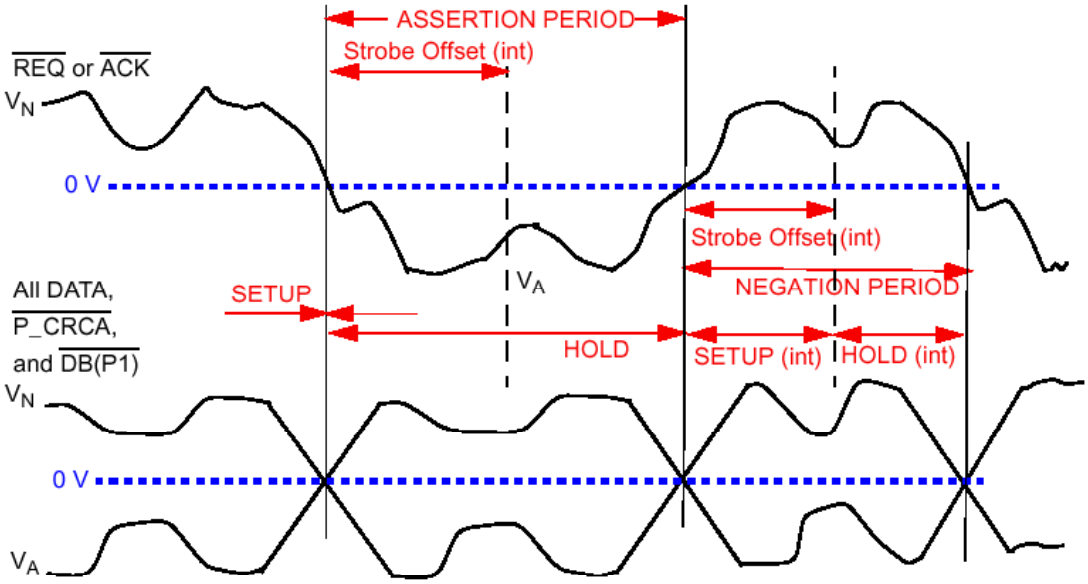
Figure 1.23 LVD DT Data Transfer measurement point

Notes:

1. V_N - negated signal
2. V_A - asserted signal
3. t_m = 1.25ns minimum
4. V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.
5. Differential voltage signals in all cases.
6. t_{af} and t_{ar} shall be less than 3 ns.
7. Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

(5) LVD Paced Transfer

Fig.1-24 is the LVD Paced Transfer measurement point.



V_N - negated signal
V_A - asserted signal
int = A value that is not observable at the SCSI connector.
Differential voltage signals in all cases.
Strobe Offset is from the actual detected time to the implemented offset time. Since effective timing is based upon actual detection, all timing measurements shall be based upon zero crossings for all paced transfers.

Figure 1.24 LVD mode DT paced transfer easurement point

1.6 Bus Phases

The SCSI bus must be in one of the following eight phases:

- BUS FREE phase
- ARBITRATION phase
- SELECTION phase
- RESELECTION phase
- COMMAND phase
- DATA phase
- STATUS phase
- MESSAGE phase

COMMAND phase, DATA phase, STATUS phase, and MESSAGE phase: INFORMATION TRANSFER phase

The SCSI bus can never be in more than one phase at any given time.

Note:

In the following bus phase conditions, signals are false unless otherwise defined. Signals on the timing charts are assumed to be positive logic (or active high).

1.6.1 BUS FREE phase

All SCSI devices do not use the bus in the BUS FREE phase. SCSI devices shall detect the BUS FREE phase after SEL and BSY signals are both false for one Bus Settle Delay.

SCSI devices which have detected the BUS FREE phase shall release all bus signals within one Bus Clear Delay after BSY and SEL signals become false for Bus Settle Delay. If a SCSI device requires more than Bus Settle Delay to detect the BUS FREE phase, it shall release all bus signals within the following period (t):

t = Bus Clear Delay - Period required for BUS FREE phase detection + Bus Settle Delay

The maximum time allowed for releasing the bus after both SEL and BSY becomes false is Bus Settle Delay + Bus Clear Delay.

Figure 1.25 shows the BUS FREE phase.

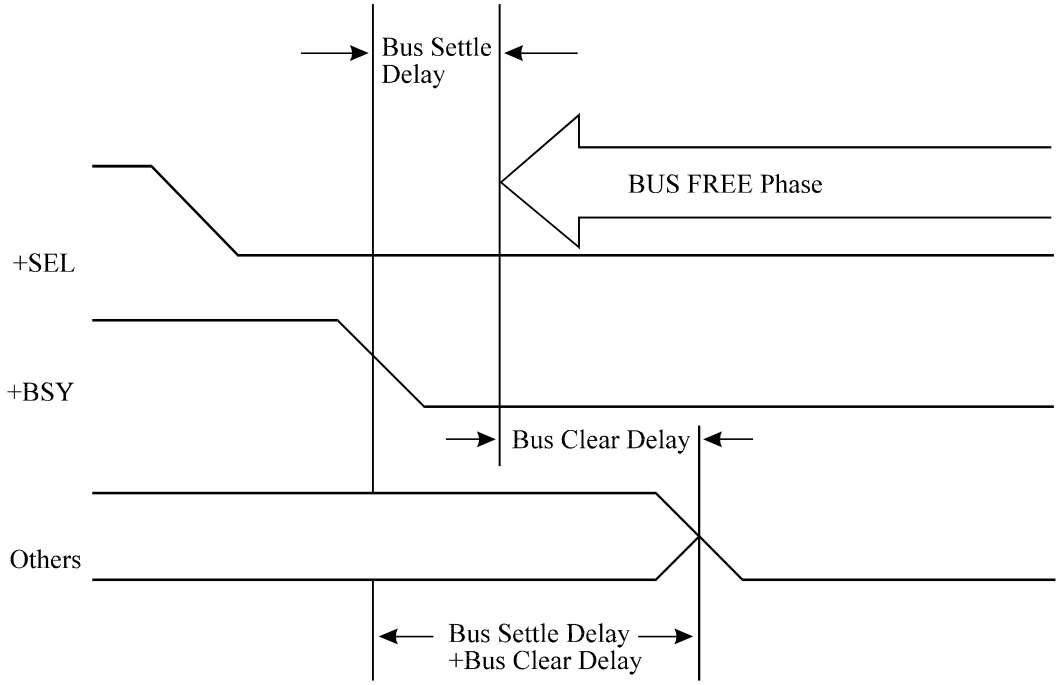


Figure 1.25 BUS FREE phase

The SCSI bus enters the BUS FREE phase when the TARG stops the BSY signal in one of the following events:

- When RESET condition has been detected.
- When TARG has received the following message normally.

  ABORT TASK, ABORT TASK SET, CLEAR TASK SET,

  LOGICAL UNIT RESET, TARG RESET, CLEAR ACA
- When TARG has transmitted the following message normally.

  DISCONNECT, TASK COMPLETE
- When a transceiver mode change.
- When the release of the SEL signal after a SELECTION or RESELECTION phase time-out.

In any case other than above, if the TARG negates the BSY signal to enter a BUS FREE phase, the TARG informs the INIT that it has detected an ERROR condition of the SCSI bus. The TARG can enter a BUS FREE phase forcibly regardless of ATN signal status; the INIT must treat that phase transition as indicating the abnormal end of command. The TARG clears all hold data or status and terminates the command being executed. It can then create sense data indicating the detailed error condition. If the INIT detects a BUS FREE phase when it is not expected, it should issue a REQUEST SENSE command to read the sense data.

1.6.2 ARBITRATION phase

1.6.2.1 Normal ARBITRATION

The ARBITRATION phase allows one SCSI device to gain control of the SCSI bus. The SCSI device that gets control of the SCSI bus can start the operation as INIT or TARG.

This is an optional system bus phase. This phase is required for the system that has two or more INITs or uses the RESELECTION phase.

Arbitration is mandoratory and requires the detection of a Bus Free phase on the SCSI bus before starting.

SCSI device with arbitration fairness enabled shall maintain a fairness register which records the SCSI IDs of devices that need a chance to arbitrate. (see 1.12).

Fairness in arbitration is enabled in targets by the Disconnect-Reconnect mode page.

Figure 1.26 shows the ARBITRATION phase, and the following explains how the SCSI device gets control of the SCSI bus.

1) The SCSI device shall wait for BUS FREE phase. (see Section 1.6.1).

2) The SCSI device shall wait at least Bus Free Delay after the BUS FREE phase detection before driving any signal.

3) Then the SCSI device that arbitrates the bus asserts the DATA BUS bit corresponding to its own SCSI ID and BSY signal (*1) within Bus Set Delay after the last observation of the BUS FREE phase.

4) After waiting at least Arbitration Delay since the SCSI device asserted BSY signal, the SCSI device shall examine the value on the DATA BUS to determine the priority of the bus arbitration (*1).

   Bus arbitration priority: DB7 (ID#7) > DB6 (ID#6) >... >DB0 (ID#0) >DB15 (ID#15) >DB14 (ID#14) >... >DB8 (ID#8)

   - When the SCSI device detects any ID bit which is assigned higher priority than its own SCSI ID, the SCSI device shall release its signals (BSY and its SCSI ID) then may return to step (1).

   - The SCSI device which detects no higher SCSI ID bit on the DATA BUS can obtain the bus control, then it shall assert SEL signal.

   - Any other SCSI device that is participating in the ARBITRATION phase shall release its signals within Bus Clear Delay after SEL signal becomes true, then may return to step (1).

5) The SCSI device which wins arbitration shall wait at least Bus Clear Delay + Bus Settle Delay after asserting SEL signal before changing any signal state.

*1: When an SCSI device sends its SCSI ID to the DATA BUS, it asserts only the bit at the position corresponding to its own ID and leaves the other or fifteen bits false. The parity bit (DBP_CRCA or DBP1 signal) may be released or asserted, but must not be actively driven false. The parity bit on the DATA BUS is unpredictable during an ARBITRATION phase.

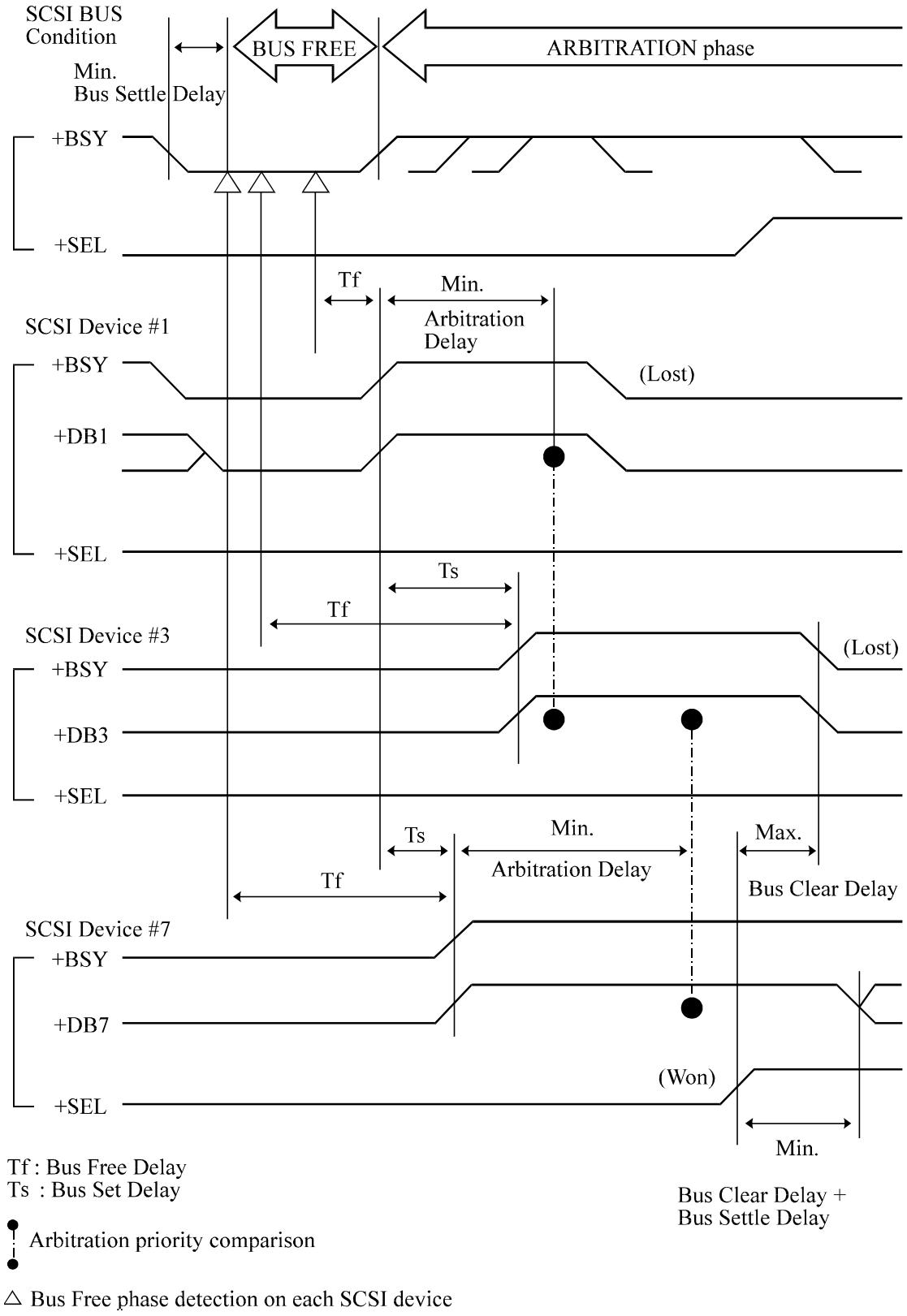


Figure 1.26 ARBITRATION phase

1.6.2.2 QAS ARBITRATION

(1) QAS protocol

QAS allows a TARG with an information unit transfer agreement in effect and QAS enabled (see 2.3.22 that is currently connected to an INIT that has QAS enabled to transfer control of the bus to another SCSI device that has QAS enabled without an intervening BUS FREE phase. SCSI devices that participate in QAS arbitration shall report that capability in the INQUIRY command.

Before the INIT may use QAS that INIT shall negotiate, using the PPR message, the use of the QAS phase with each TARG that has indicated support of QAS. Any time the INIT's negotiation required flag is true (see 4.12) that INIT shall renegotiate to enable QAS. SCSI devices that support QAS shall implement the fairness algorithm (see 1.13) during all QAS arbitrations. SCSI devices shall negotiate the use of QAS with a particular SCSI device before using QAS to select or reselect that SCSI device. Also, TARG shall have negotiated the use of QAS with a particular INIT before using QAS REQUEST message to do a physical disconnect from that INIT, and INIT shall have negotiated the use of QAS with a particular TARG before accepting a QAS REQUEST message from that TARG. If the INIT receives a QAS REQUEST message from a TARG that has not negotiated the use of QAS, then the INIT shall create an attention condition for the QAS REQUEST message, and shall report MESSAGE REJECT on the following MESSAGE OUT phase.

In an environment where some SCSI devices have QAS enabled and other SCSI devices do not, it is possible for the SCSI devices that have QAS enabled to prevent SCSI devices that do not have QAS enabled from arbitrating for the bus. This occurs when SCSI devices that have QAS enabled never go to a BUS FREE phase.

A QAS INIT may interrupt a sequence of QAS cycles to force a normal arbitration with the following procedure:

1) Perform a QAS arbitration;
2) On winning QAS arbitration, continue driving the INIT ID on the DATA BUS instead of asserting SEL to enter selection phase;
3) Wait until the TARG transitions to BUS FREE (i.e., after two QAS arbitration delays);
4) After detecting BSY false, release the DATA BUS; and
5) After one bus settle delay from when the TARG drove BSY false, the bus is in BUS FREE phase. The INIT port may then arbitrate using normal arbitration and perform a selection if it wins.

(2) QAS phase

The procedure for a TARG with both information unit transfers and QAS enabled to Indicate it wants to release the bus after a DT DATA phase is as follows:

1) The TARG changes to a MESSAGE IN phase and issue a single QAS REQUEST message (see 2.3.22) and wait for ACK to be true.
2) After detection of the ACK signal being false and if the INIT did not create an attention condition, the TARG releases all SCSI signals except the BSY, MSG, C/D, I/O, and REQ signals. Then the TARG negates the MSG, C/D, and I/O signals within two system deskew delays. The TARG waits two system deskew delays after negating the C/D, I/O, and MSG signals before releasing the REQ signal.
3) If the INIT did not create an attention condition then the INIT shall release all SCSI signals except ACK and ATN within two system deskew delays after detecting MSG, C/D, and I/O signals false.

4) If the INIT creates an attention condition then the TARG will go to a MESSAGE OUT phase, receive all the message bytes, and cause an unexpected bus free by generating a BUS FREE phase.
5) If the TARG detects the SEL signal being true, the TARG will release the BSY, MSG, C/D, and I/O signals within one QAS release delay.
6) After waiting at least one QAS arbitration delay from negating the SCSI MSG, C/D, and I/O signals in step 2), if there are no SCSI ID bits true the TARG will transition to the BUS FREE phase.
7) After waiting at least one QAS arbitration delay from negating the MSG, C/D, and I/O signals in step 2), if there are any SCSI ID bits true the TARG will wait at least a second QAS arbitration delay. If the SEL signal is not true by the end of the second QAS arbitration delay the TARG transitions to the BUS FREE phase.

Note :

The release of MSG, C/D, and I/O may cause release glitches; Step 5) above ensures these glitches occur at a time when no connection is established on the bus so that they do not interfere with proper operation.

The procedure for a SCSI device with QAS enabled to obtain control of the SCSI bus via QAS is as follows:

1) The SCSI device shall first wait for MESSAGE IN phase to occur following a DT DATA phase with a single QAS REQUEST message. When the SCSI device detects the ACK signal being false for the QAS REQUEST message and the attention condition is cleared it shall begin the QAS phase.
2) The SCSI device shall wait a minimum of two system deskew delays after detection of the MSG, C/D, and I/O signals being false before driving any signal.
3) Following the delay in step 2), the SCSI device may arbitrate for the SCSI bus by asserting its own SCSI ID within one QAS assertion delay from detection of the MSG, C/D, and I/O signals being false. If arbitration fairness is enabled, the SCSI device shall not arbitrate until its fairness register is cleared.
4) After waiting at least one QAS arbitration delay, measured from the detection of the MSG, C/D, and I/O signals being negated, the SCSI device shall examine the DATA BUS.

   A) If no higher priority SCSI ID bit is true on the DATA BUS and the fairness algorithm allowed the SCSI device to participate, then the SCSI device has won the arbitration and it shall assert the SEL signal.

   B) If a higher priority SCSI ID bit is true on the DATA BUS or the fairness algorithm prevented the SCSI device from participating in QAS arbitration, then the SCSI device has lost the arbitration.

   C) Any SCSI device other than the winner has lost the arbitration and shall release its SCSI ID bit after two system deskew delays and within one QAS release delay after detection of the SEL signal being true. A SCSI device that loses arbitration may return to step 1).

5) The SCSI device that wins arbitration shall wait at least one QAS arbitration delay after asserting the SEL signal before changing any signals.
6) After the QAS arbitration delay in step 4), SCSI devices with arbitration fairness enabled that are not arbitrating shall start sampling the DATA BUS to determine the SCSI devices that are attempting arbitration, the SCSI device that won, and the SCSI devices that lost. This sampling shall continue for one bus settle delay plus two system deskew delays. The SCSI devices shall update their fairness register with all device IDs that lost arbitration.

The SCSI ID bit is a single bit on the DATA BUS that corresponds to the SCSI device's unique SCSI address. All other DATA BUS bits shall be released by the SCSI device. The DB(P_CRCA) and DB(P1) are not valid during the QAS phase. During the QAS phase, DB(P_CRCA), and DB(P1) may be released or asserted, but shall not be actively driven false.

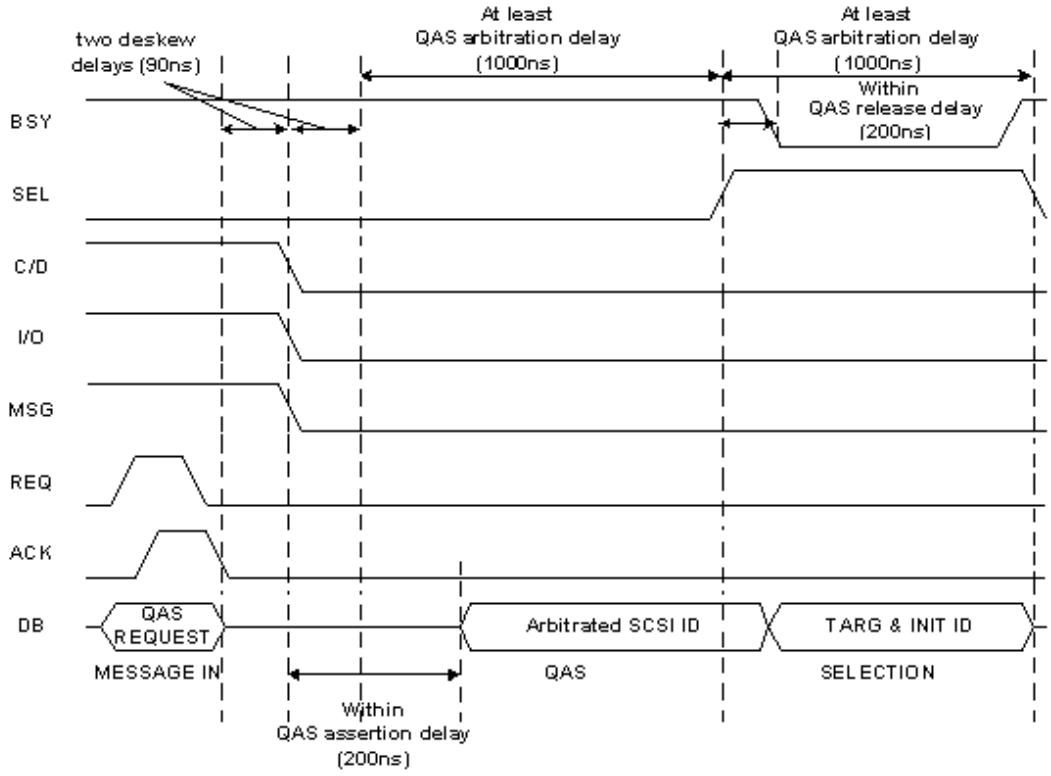


Figure 1.27 QAS phase

1.6.3 SELECTION phase

An INIT selects a TARG (a single SCSI unit) in the SELECTION phase.

Note:

I/O signal is false during a SELECTION phase. (The I/O signal identifies the phase as SELECTION or RESELECTION).

(1) Start sequence without ARBITRATION phase

In systems with the ARBITRATION phase not implemented, the INIT starts the SELECTION phase in the following sequence (see Figure 1.28).

1) The INIT shall wait for at least Bus Clear Delay after BUS FREE phase detection.

2) Then the INIT asserts SCSI IDs of desired TARG and INIT itself on the DATA BUS.

Note:

If single INIT operates without the RESELECTION phase, it is allowed to assert only the TARG's SCSI ID.

3) After waiting at least Deskew Delay × 2, the INIT asserts SEL signal and waits the response (BSY signal) from the TARG.

(2) Start sequence with ARBITRATION phase

In systems with ARBITRATION phase implemented, the INIT starts the SELECTION phase in the following sequence (see Figure 1.28).

1) The INIT shall wait for at least Bus Clear Delay + Bus Settle Delay after turning SEL signal on during the ARBITRATION phase.

2) Then the INIT asserts SCSI IDs of the desired TARG and INIT itself on the DATA BUS.

Note:

If single INIT operates without RESELECTION phase, it is allowed to assert only the TARG's SCSI ID.

3) The INIT releases BSY signal after waiting at least Deskew Delay × 2. The INIT shall then wait at least Bus Settle Delay before looking for the response (BSY signal) from the TARG.

(3) Selection enabled parity protection and using/without using attention condition

1) The INIT sets the DATA BUS to a value that is the OR of INIT's SCSI ID bit, the TARG's SCSI ID bit, and the appropriate parity bit(s) (i.e., DB(P_CRCA and/or P1)).

2) In the case of selection using attention condition, the INIT should create an attention condition (indicating that a MESSAGE OUT phase is to follow the SELECTION phase).
But in the case of selection without using attention condition, the INIT should clear an attention condition

3) The INIT waits at least two System Deskew Delays and releases the BSY signal.

4) The INT then wait at least one Bus Settle Delay before attempting to detect an assertion of the BSY signal from the TARG.

(4) Response sequence

When an SCSI device (TARG) detects that the SEL signal and the data bus bit (DBn) corresponding to the own SCSI ID are true and both BSY and I/O signals are false for at least Bus Settle Delay, the SCSI device shall recognize that it is selected in the SELECTION phase. At this time, the selected TARG may sample all bits on the SCSI bus to identify the INIT's SCSI ID.

The TARG must response to the INIT by asserting the BSY signal within Selection Abort Time since the TARG detects that the TARG is selected. If the SCSI ID with three or more bits is detected, or if a parity error is detected under the system that the parity bit is enabled, the TARG shall not respond to the SELECTION phase.

At least Deskew Delay × 2 after the BSY signal (asserted by the TARG) detection, the INIT shall release SEL signal. The values on the DATA BUS can be changed after this time.

Note:

When Selection without using attention condition, if an INIT detects an unexpected COMMAND phase, it invalidates all prior negotiations with the selected TARG.

In this case, the INIT should create an attention condition and on the corresponding MESSAGE OUT phase should issue an ABORT TASK message.

On the next selection of the TARG that received the ABORT TASK message the INIT should do a selection using the attention condition.

With using attention condition, if an information unit transfer agreement is in effect for the connecting INIT the TARG proceeds to a MESSAGE OUT phase. If the first message received by the TARG during the MESSAGE OUT phase is not a TARGET RESET message or a PPR message the TARG will change to a MESSAGE IN phase and issue a MESSAGE REJECT message then originate WDTR negotiation with the TRANSFER WIDTH EXPONENT field set to 00h.

(5) Timeout procedure

If the INIT cannot detect the response from TARG when the Selection Timeout Delay or longer has passed after starting the SELECTION phase, the timeout procedure shall be performed through one of the following schemes:

a) The case of creating Reset condition
The INIT should assert the RST signal.

b) The case of no response from the selected TARG

1) The INIT should continue asserting the SEL signal.

2) If the INIT creates an attention condition, The INIT should keep ATN signal asserted.

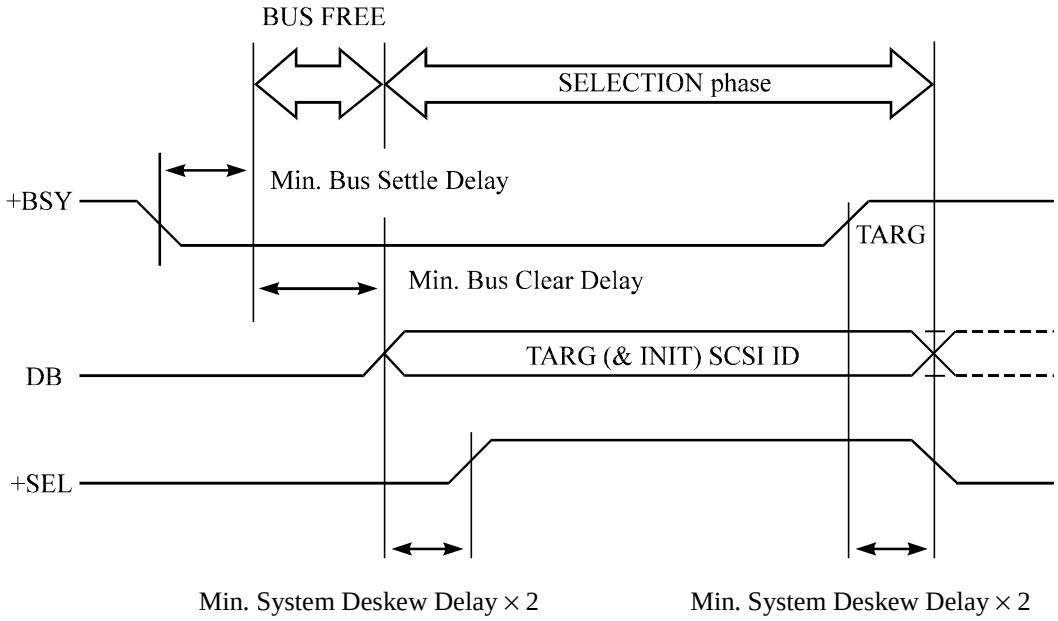
3) The INIT should release DB(15-0,P_CRCA,and/or P1).

4) If the INIT has not detected the BSY signal to be true after at least one Selection Abort Time plus two System Deskew Delays, the INIT should release the SEL signal and ATN signal (if Selection using attention condition) allowing the SCSI bus to go to the BUS FREE phase.

5) SCSI devices should ensure that when responding to selection was still valid within one Selection Abort Time of their assertion of the BSY signal.

6) Failure to comply with this requirement could result in an improper selection (two TARG connected to the same INIT, wrong TARG connected to an INIT, or a TARG connected to no INIT).

(System that does not use the ARBITRATION phase)



(System that use the ARBITRATION phase)

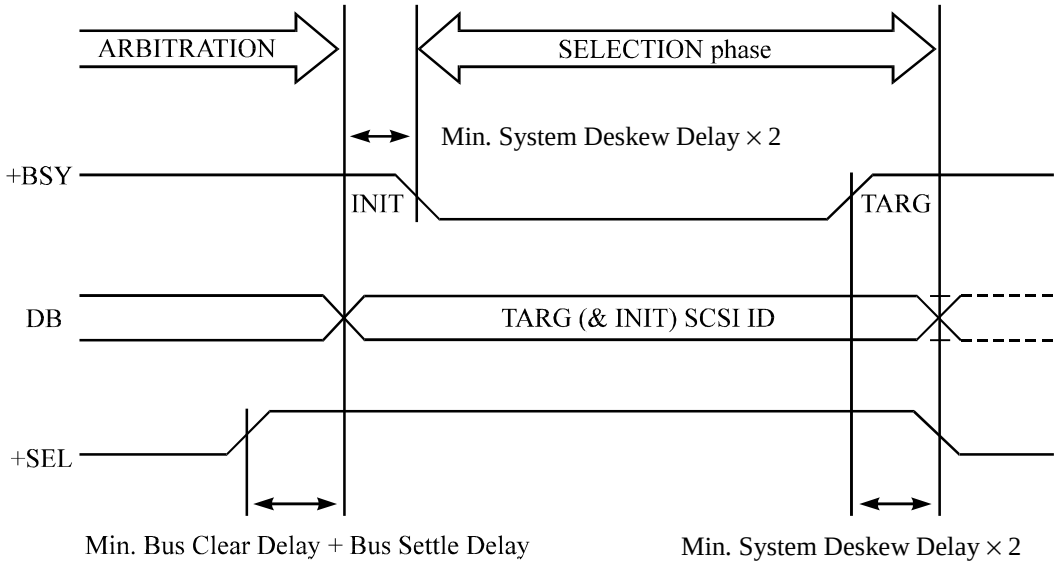


Figure 1.28 SELECTION phase

1.6.4 RESELECTION phase

The SCSI device operated as a TARG selects an INIT in the RESELECTION phase. This phase is an option for the system, and this phase can only be used in systems with the ARBITRATION phase implemented.

When the TARG re-starts the command processing under the disconnection on the SCSI bus, the TARG reconnects with the INIT using this phase.

(1) Start sequence

A TARG performs the RESELECTION phase in the following sequence after obtaining control of the SCSI bus through the ARBITRATION phase (see Figure 1.29).

(a) Parity Protection is disabled

1) TARG waits at least Bus Clear Delay + Bus Settle Delay after asserting the SEL signal in the ARBITRATION phase.

2) The TARG asserts the I/O signal with sending the SCSI IDs of the TARG itself and INIT to the SCSI bus (the SCSI device that gets the bus usage right by asserting the I/O signal is recognized as a TARG).

3) The TARG releases the BSY signal after waiting at least Deskew Delay $\times$ 2, and the TARG shall then wait the response (BSY signal) from the INIT after at least Bus Settle Delay passed.

(b) Parity Protection Enabled

1) The SCSI device that won arbitration has both the BSY and SEL signals asserted and has delayed at least one Bus Clear Delay plus one Bus Settle Delay before ending the ARBITRATION phase.

2) The SCSI device that won arbitration identifies itself as a TARG by asserting the I/O signal.

3) The TARG also sets the DATA BUS to a value that is the logical OR of TARG's SCSI ID bit, the INIT's SCSI ID bit and the appropriate parity bit(s).

4) The TARG waits at least two System Deskew Delays and releases the BSY signal.

5) The TARG then waits at least one Bus Settle Delay before attempting to detect an assertion of the BSY signal by the INIT.

(2) Response sequence

If a SCSI unit (INIT to be selected) detects the SEL and I/O signals and data bus bit (DBn) corresponding to the own SCSI ID are all true and if it detects the BSY signal which is false for at least Bus Settle Delay, the SCSI unit shall recognize that it is selected in the RESELECTION phase. At this time, the selected INIT samples all bits on the data bus to identify the TARG's SCSI ID.

The INIT shall respond to the TARG by asserting the BSY signal within Selection Abort Time from the INIT detects that it is selected.

If the SCSI ID in other than two or bits is detected on the data bus or if a parity error is detected on the system where the parity bit is enabled on the data bus, the INIT shall not respond to the RESELECTION phase.

When TARG detects the response (BSY signal) from INIT, the TARG asserts BSY signal and waits at least Deskew Delay × 2, then the TARG releases SEL signal. At this time, the TARG may change the I/O signal state and value on the SCSI bus.

The INIT shall release the BSY signal after making sure that the SEL signal becomes false.

The TARG should continue asserting the BSY signal until the TARG relinquishes the SCSI bus.

Note:

When the TARG is asserting the BSY signal, a transmission line phenomenon known as a wired-OR glitch may cause the BSY signal to appear false for up to a round-trip propagation delay following the release of the BSY signal by the INIT.

This is the reason why the BUS FREE phase is recognized only after both the BSY and SEL signals are continuously false for a minimum of one Bus Settle Delay.

(3) Timeout procedure

If the TARG cannot detect a response (BSY signal) from the INIT when the Selection Timeout Delay or longer has passed after starting the RESELECTION phase, the timeout procedure shall be performed though one of the following schemes:

1) The TARG asserts the TRUE signal and generates an RESET condition.

2) The INIT maintains SEL and I/O signals true and stops sending the SCSI ID to the data bus. Subsequently, the INIT waits for the response from TARG for at least Selection Abort Time + Deskew Delay × 2. If no response is detected, the INIT releases the SEL and I/O signals allowing the SCSI bus to go to the BUS FREE phase. If the INIT detects the response from the TARG during this period, the INIT considers the SELECTION phase to have completed normally.

The IDD performs process 2) above as RESELECTION phase time-out processing.

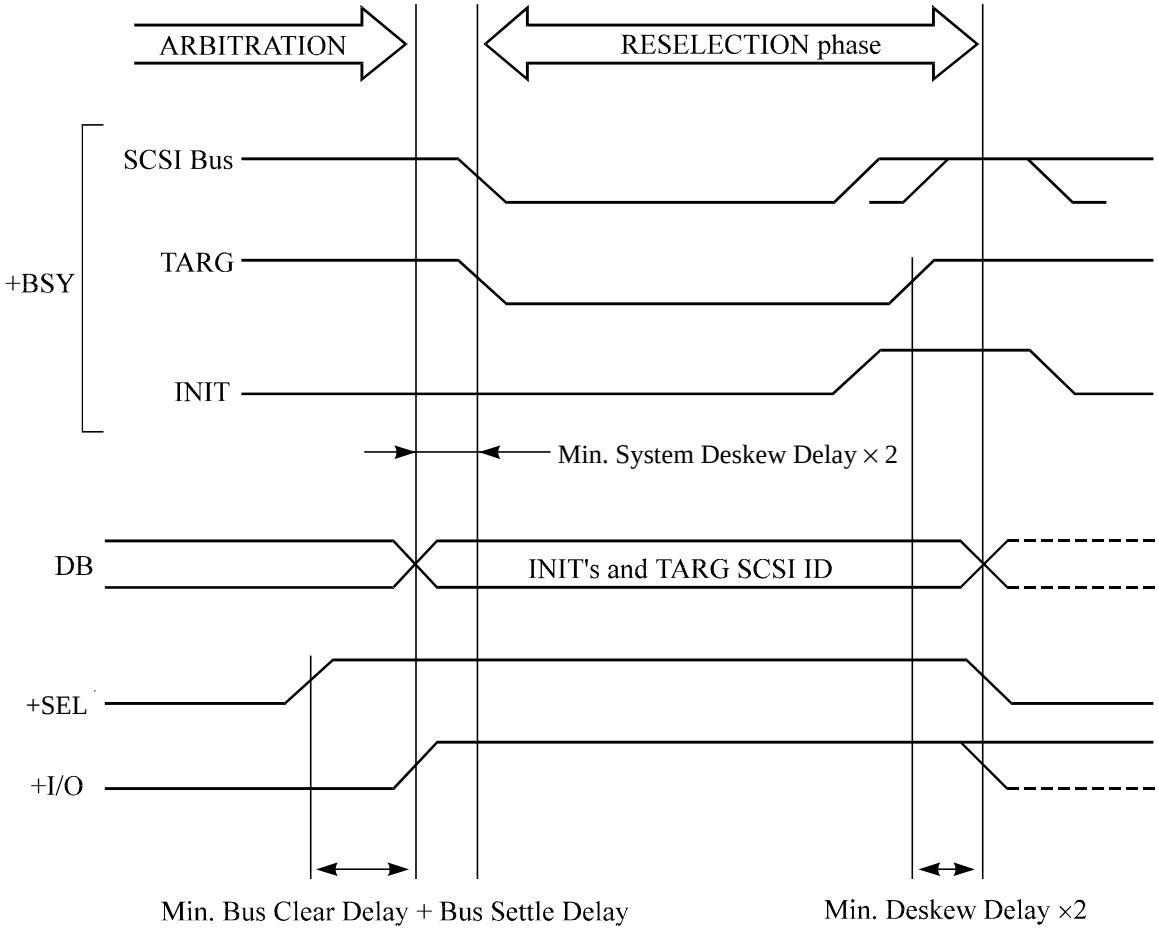


Figure 1.29 RESELECTION phase

1.6.5 INFORMATION TRANSFER phases

The COMMAND, DATA, STATUS and MESSAGE phases are generally called the INFORMATION TRANSFER phase. This phase can transfer the control information and data between the INIT and TARG via the data bus.

The type of INFORMATION TRANSFER phase is determined by the combination of C/D, I/O, and MSG signals (see Table 1.1). Since these three signals are specified by the TARG, phase transition is controlled by the SCSI device operating as a TARG. The INIT can request the TARG to initiate a MESSAGE OUT phase by sending an ATN signal. Besides, the TARG can change the bus phase to BUS FREE by ceasing the transmission of BSY signal.

During INFORMATION TRANSFER phase, the information transfer is controlled by the REQ and ACK signals. The TARG sends the REQ signal to request for information transfer, and the INIT responds to it with the ACK signal. A pair of REQ and ACK signals is used to transfer a single-byte information on the 8-bit SCSI bus or two-byte information on the 16-bit SCSI bus. There are two types of information transfer modes: synchronous and asynchronous transfer modes. They differ from each other by their REQ signal transmission and ACK signal response methods (called the REQ/ACK handshaking). Also, the 16-bit SCSI bus can transfer 16-bit wide data only in the DATA phase.

The 16-bit SCSI bus can transfer 16-bit wide data only in the DATA phase except alternate error detection for the asynchronous information phase (COMMAND, MESSAGE and STATUS). The detail of these phase is described below section.

The target shall not transition into an information transfer phase unless the REQ/ACK signals are negated. The target shall not transition from an information transfer phase into another information transfer phase unless the REQ/ACK signals are negated. During INFORMATION TRANSFER phase, the TARG shall keep the BSY signal true but keep the SEL signal false. The TARG shall establish the status of C/D, I/O and MSG signals (which determine the phase type) at least Bus Settle Delay before the leading edge of REQ signal which requests to transfer the first byte. The TARG shall keep the status until it detects the trailing edge of the ACK signal which corresponds to the last byte in that phase (see Figure 1.30).

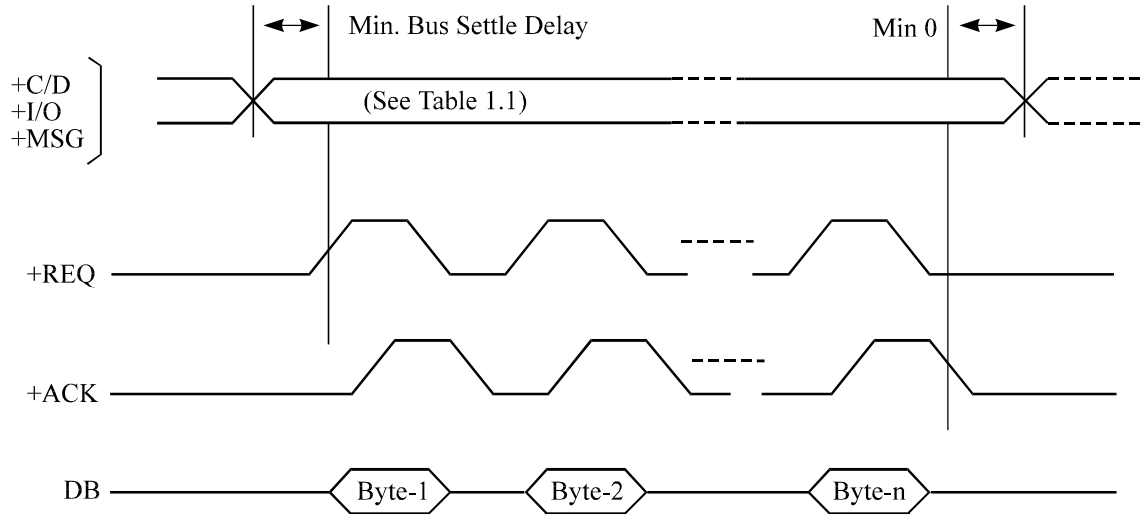


Figure 1.30 INFORMATION TRANSFER phase (phase control)

Notes:

1. After the ACK signal becomes false in the current INFORMATION TRANSFER phase, the TARG can start preparing a new phase by changing the status of C/D, I/O and MSG signals. The status of these three signals can change in any order or at once. The status of one signal may change more than once; however, the TARG should change the status of each signal only once.

2. A new INFORMATION TRANSFER phase starts when the REQ signal requesting to transfer the first byte in that phase becomes true. The phase ends when one of C/D, I/O and MSG signals changes after the ACK signal has changed to false. The period after the end of phase to the start of next phase (which starts when the REQ signal becomes true) is not defined.

3. The INIT can predict the next new phase (expected phase) by reading the status change of C/D, I/O or MSG signal or by reading the type of previously executed phase. However, the expected phase is made valid only when the REQ signal is changed to true.

1.6.5.1 Asynchronous transfer mode

In asynchronous transfer mode, the INIT and TARG control the information transfer by checking the status change of REQ and ACK signals (between true and false state) by each other (it is called the interlock control). The asynchronous transfer can be used in all types of INFORMATION TRANSFER phase (such as COMMAND, DATA, STATUS and MESSAGE). Figure 1.31 shows the timing of asynchronous transfer.

If the wide mode data transfer is established between the INIT and TARG, the two-byte data (DB15 to DB0, DBP1, DBP_CRCA) is transferred on the 16-bit SCSI bus. Otherwise, single-byte data (DB7 to DB0, DBP_CRCA) is transferred.

a. Transfer from TARG to INIT

The TARG determines the information transfer direction by the I/O signal. If the I/O signal is true, the information of the data bus is transferred from the TARG to the INIT. The following explains the information transfer sequence.

1) The TARG asserts the REQ signal at least one System Deskew Delay + Cable Skew Delay after sending valid information on the data bus. It must maintain the state of the data bus until the ACK signal becomes true on the TARG.

2) The INIT fetches the data from the data bus after the REQ signal becomes true. It asserts the ACK signal to report the completion of reception.

3) After the ACK signal becomes true on the TARG, the TARG negates the REQ signal and the TARG may change or release the DB(7-0, P_CRCA) or DB(15-0, P_CRCA, P1) signals.

4) The INIT negates the ACK signal after the REQ signal becomes false.

5) After the ACK signal becomes false, the TARG proceeds to the next byte transfer stage.

b. Transfer from INIT to TARG

When the I/O signal is false, the information of the data bus is transferred from the INIT to the TARG. The following explains the information transfer sequence.

1) The TARG asserts the REQ signal to request the INIT for information transfer.

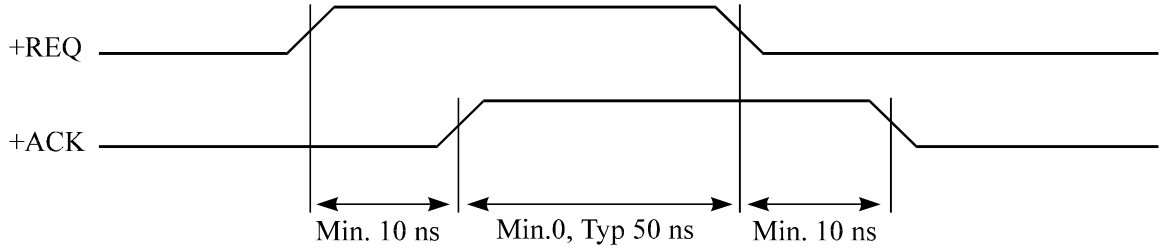
2) The INIT asserts the ACK signal at least one System Deskew Delay + Cable Skew Delay after sending valid information of the requested type on the data bus. The information on the data bus must be maintained until the REQ signal becomes false on the INIT.

3) The TARG fetches data from the data bus after the ACK signal becomes true, and negates the REQ signal to report the completion of reception.

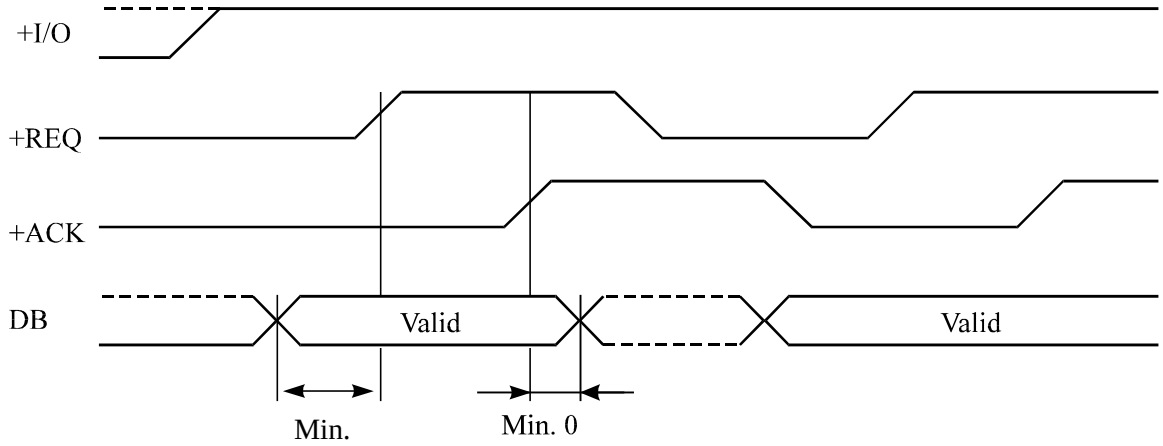
4) When the REQ signal becomes false on the INIT, the INIT negates the ACK signal. After that, the INIT may release or change the DB(7-0, P_CRCA) or DB(15-0, P_CRCA, P1) signals.

5) After the ACK signal becomes false, the TARG proceeds to the next byte transfer stage.

[Timing rule for REQ and ACK signals]
Note: Time is defined on SCSI connector pins on the IDD.

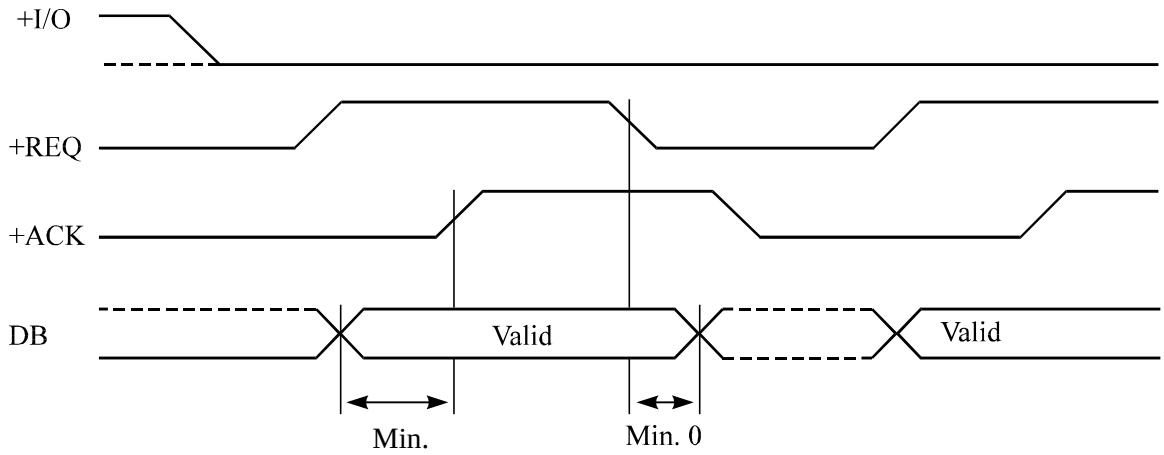


[Timing rule for TARG to INIT]
Note: Time is defined on SCSI connector pins on the TARG.



System Deskew Delay + Cable Skew Delay

[Timing rule for INIT to TARG]
Note: Time is defined on SCSI connector pins on the TARG.



System Deskew Delay + Cable Skew Delay

Figure 1.31 Transfer in asynchronous mode

c. Improved Error Detection for the Asynchronous Information Phases (AIP)

The COMMAND, MESSAGE and STATUS asynchronous information transfer phases except DATA phase only transfer information on the lower eight data bits of a SCSI bus with only normal parity protection on those transfers. In this improved detection additional check information can be transferred on the upper eight data bits. This error detection can improve error detection capabilities. Since the upper eight data bits of the SCSI bus are used for this scheme, this error detection method is only available on wide SCSI devices that are on wide SCSI buses.

The additional check information is called "protection code". This code contains 21-bit code word and covered signals of the 16-bit SCSI data bus. Protection code checking is enabled or disabled on an I_T nexus basis. Protection code checking is disabled in the following case:
- After a power cycle
- After a hard reset
- After a TARGET RESET message
- After a change in the transceiver mode (i.e, LVD mode to MSE mode)

A SCSI device enable protection code checking for an I_T nexus when it detects that valid protection code data is being transmitted on the upper byte of the SCSI bus. The following are some possible times when a SCSI device could try to enable protection code checking:
- During the first COMMAND, MESSAGE or STATUS phase
- After a UNIT ATTENTION condition
- During the MESSAGE phase of a negotiation

Protection code errors are handled exactly parity errors during COMMAND, MESSAGE or STATUS phases. But this parity error outputs will be logically OR'd into the existing parity error logic. There are the some kinds of "parity error" as follows:
- DT mode CRC error
- DBP1, DB15-8 negated
- DBP1, P_CRCA parity error
- Protection code error

The kind of parity error isn't determined and when the device detected parity error, the device proceeds to the next procedure without retry. The detail of the procedure is discribed in CHAPTER 3, ERROR RECOVERY.

1.6.5.2 Synchronous mode

Synchronous data transfer is optional and is only used in DATA phases. It shall be used in a DATA phase if a synchronous data transfer agreement has been established. The agreement specifies the REQ/ACK offset and the minimum transfer period.

When synchronous data transfers are being used data may be transferred using ST data transfers or, optionally, DT data transfers. DT data transfers shall only be used on 16 bit wide buses that transmit and receive data using LVD transceivers.

The synchronous transfer mode allows information transfer with REQ and ACK signal check by their pulse count (called the offset interlock). This mode can be used in the DATA phase only.

Note:

1. The IDD supports up to 20 MHz (40 MHz on LVD) of synchronous data transfer (see Table 1.7).

2. The default data transfer mode is asynchronous. When the power is first turned on, the system is reset, or after the TARGET RESET message has been issued, data is transferred in the asynchronous mode only. It continues until the synchronous transfer mode is selected by the message exchange explained below.

(1) ST synchronous data transfer

The ST synchronous data transfer is available only when it has been defined between the INIT and TARG by exchanging the SYNCHRONOUS DATA TRANSFER REQUEST or PARALLEL PROTOCOL REQUEST message with each other. The following data transfer parameters are determined and the possible transfer rate between the SCSI units are defined by this message exchange.

- REQ/ACK Offset: Number of REQ signals that the TARG can send before receiving the ACK signal.

- Transfer Period: Minimum repetition cycle of REQ and ACK signals.

The TARG can send multiple REQ signal pulses before receiving an ACK signal response if these pulses do not exceed the limit specified by the REQ/ACK Offset parameter. When the difference between the REQ and ACK signal pulses has reached this limit at the TARG, the TARG shall not send a REQ pulse until it receives the leading edge of the next ACK pulse. The data transfer in DATA phase can complete normally only when the REQ and ACK signal pulses become equal to each other.

(a) The case of the I/O signal is true (transfer to the INIT)

1) The TARG first drives the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals to their values.

2) The TARG waits at least one Transmit Setup Time.

3) The TARG asserts the REQ signal.

4) The DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals are held valid for a minimum of one Transmit Hold Time after the assertion of the REQ signal.

5) The TARG asserts the REQ signal for a minimum of one Transmit Assertion Period.

6) The TARG may then negate the REQ signal and change or release the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals.

7) The INIT reads the value on the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals within one Receive Hold Time of the transition of the REQ signal to true.

8) The INIT then responds with an ACK assertion.

(b) The case of the I/O signal is false (transfer to the TARG)

1) The INIT detects a REQ assertion.

2) The INIT first drives the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals to their values.

3) The INIT delays at least one Transmit Setup Time.

4) The INIT asserts the ACK signal.

5) The INIT holds the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals valid for at least one Transmit Hold Time after the assertion of the ACK signal.

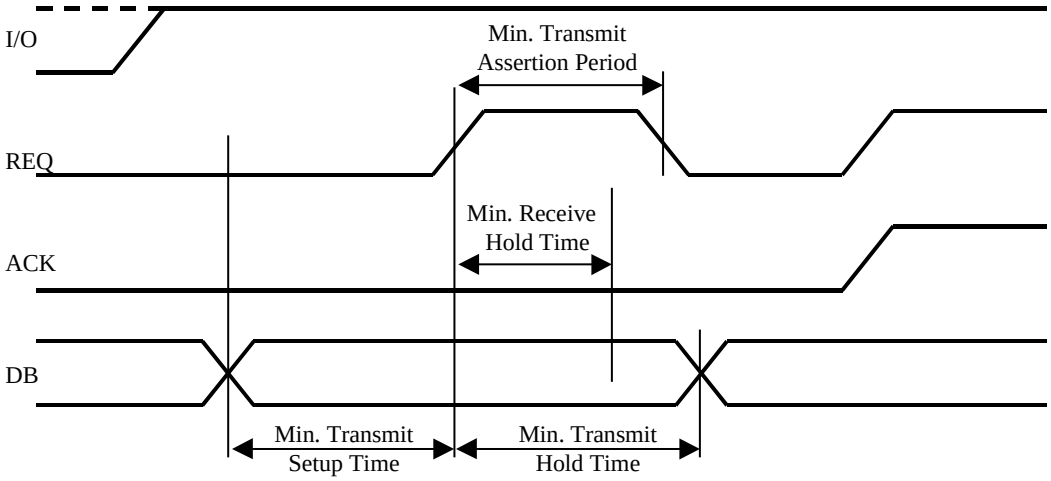
6) The INIT asserts the ACK signal for a minimum of one Transmit Assertion Period.

7) The INIT may then negate the ACK signal and change or release the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals.

8) The TARG reads the value of the DB(7-0,P_CRCA) or DB(15-0,P_CRCA,P1) signals within one Receive Hold Time of the transition of the ACK signal to true.

Figure 1.32 shows the timing requirements for ST synchronous mode.

[Timing rule for TARG to INIT]



[Timing rule for INIT to TARG]

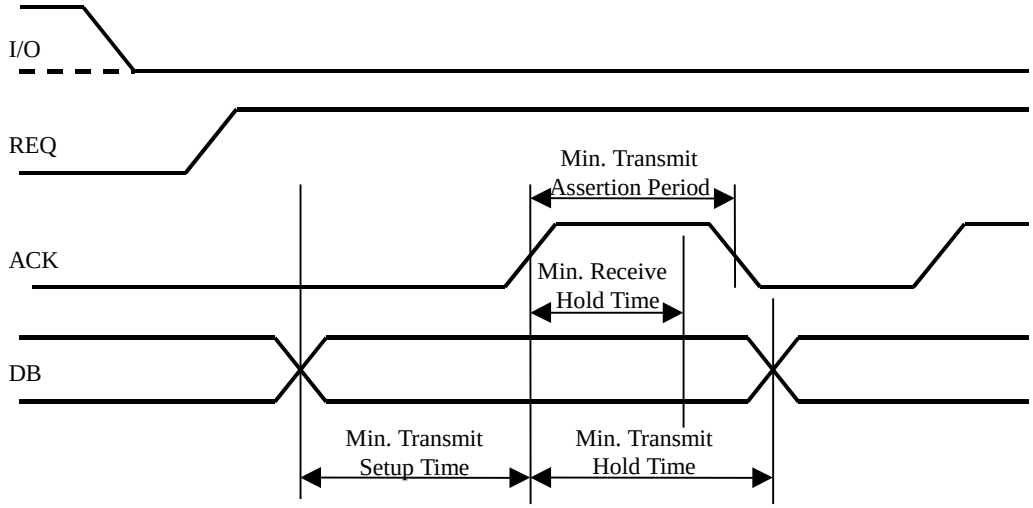


Figure 1.32 ST transfer in synchronous mode

(2) DT synchronous data transfer

When a DT data transfer agreement has been established the target shall only use the DT DATA IN phase and DT DATA OUT phase for data transfers. The DT synchronous data transfer is available only when it has been defined between the INIT and TARG by exchanging the PARALLEL PROTOCOL REQUEST message with each other.

During DT data transfers data shall be clocked on both the assertion and negation of the REQ and ACK signal lines. References to REQ/ACK transitions in this subclause refer to either an assertion or a negation of the REQ or ACK signal.

The REQ/ACK offset specifies the maximum number of REQ transitions that shall be sent by the target in advance of the number of ACK transitions received from the initiator, establishing a pacing mechanism. If the number of REQ transitions exceeds the number of ACK transitions by the REQ/ACK offset, the target shall not transition the REQ signal until after the next ACK transition is received. For successful completion of the DT DATA phase the number of ACK and REQ transitions shall be equal and both REQ and ACK shall be negated.

Note:

The differences from the ST DATA Synchronous mode are the following: (ST DATA Sync Mode)

1. Only LVD, up to Fast-80 transfer (up to Fast-20, Fast-40 on LVD)
2. 16 bits transfer only (Either 8 bit or 16 bit transfer is available)
3. MSG signal is asserted (MSG signal negated)
4. P_CRCA, P1 signals are used as Data Group Transfer enabled.
5. Both edges of the REQ / ACK are available in the data transmission (Only trailing edge is available)

Data group contains three fields. They are Data field, Pad field, pCRC field. The following description is about each field transfer.

(a) Data Group Data field transfer from TARG to INIT

The TARG specifies the data transfer direction using the I/O signal. When the I/O signal is true, data is transferred from the TARG to the INIT. And MSG signal determines the kind of DATA phase. When the MSG signal is true, the DATA phase is DT DATA phase. The following explains the transmission sequence. The target shall not transition the REQ signal when the P_CRCA signal is asserted for the current data group until the initiator has responded with all ACK transitions for the previous data groups.

1) TARG drives the DB(15-0) signals to their desired values and shall negate the P_CRCA signal.
2) TARG waits at least the longer of a pCRC transmit setup time from the negation of P_CRCA or a transmit setup time from DB(15-0) signals being driven with valid data.
3) TARG transits the REQ signal and holds the DB(15-0) signals valid for a minimum of a transmit hold time and the P_CRCA signal for a minimum of a pCRC transmit hold time.
4) TARG holds the REQ signal for at least a transmit assrttion period if asserted or a transmit negation period if negated.

5) INIT fetches the values from DB(15-0) signals within a receive hold time of the transition of the REQ signal and it also fetches the value from the P_CRCA signal within a pCRC receive hold time of the transition of the REQ signal. Then INIT responds with an ACK transition.

(b) Data Group Data field transfer from INIT to TARG

When the I/O signal is false, data is transferred from the INIT to the TARG. Other condition is the same in the section (a).

1) INIT drives the DB(15-0) signals to their desired values after detecting a REQ transition with P_CRCA signal negated.

2) INIT waits at least a transmit setup time and transits ACK signal.

3) INIT holds the DB(15-0) signals valid for at least a transmit hold time and ACK signal for a minimum of a transmit assertion period if asserted or a transmit negation period if negated.

4) TARG fetches the value of the DB(15-0) signals within a receive hold time of the transition of the ACK.

(c) Data Group Pad field and pCRC field transfer from TARG to INIT

The target determines a pad field is required if the I/O signal is true, the target has completed the data field transfer of the current data group, and REQ signal is asserted. (Pad field required)

1) TARG waits at least one pCRC transmit hold time since the last REQ assertion to assert P_CRCA.

2) TARG waits at least one transmit hold time since the last REQ assertion to assert the DB(15-0) signals to their desired pad values.

3) TARG waits at least the longer of a pCRC transmit setup time from the assertion of P_CRCA or a transmit setup time from DB(15-0) being driven with valid pad data.

4) TARG waits until the initiator has responded with all ACK transitions for the previous data group.

5) TARG waits at least one transmit REQ assertion period with P_CRCA transitioning since the last REQ assertion.

6) TARG negates the REQ signal hold the DB(15-0) signals valid for a minimum of one transmit hold time and holds the REQ signal negated for a minimum of a transmit negation period.

7) TARG drives the DB(15-0) signals to their desired pCRC values and waits at least one transmit setup time.

8) TARG asserts the REQ signal and holds the DB(15-0) signals for a minimum of one transmit hold time and the REQ signal asserted for a minimum of a transmit assertion period.

9) TARG drives the DB(15-0) signals to their desired pCRC values and waits at least one transmit setup time.

10) TARG negates the REQ signal and holds the DB(15-0) signals for a minimum of one transmit hold time and the P_CRCA signal asserted for at least a pCRC transmit hold time.

11) TARG holds the REQ signal negated for at least one transmit REQ negation period with P_CRCA transitioning since the last REQ negation.

If the target determines no pad field is required, the the transmission sequence is the following way.

1) TARG waits at least one pCRC transmit hold time since the last REQ negation to assert P_CRCA.

2) TARG waits at least one transmit hold time since the last REQ negation to assert the DB(15-0) signals to their desired pCRC values.

3) TARG waits at least the longer of a pCRC transmit setup time from the assertion of P_CRCA or a transmit setup time from DB(15-0) being driven with valid pCRC data.

4) TARG waits until the INIT has responded with all ACK transitions for the previous data group.

5) TARG waits at least one transmit REQ negation period with P_CRCA transitioning since the last REQ negation.

6) TARG asserts the REQ signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the REQ signal asserted for a minimum of a transmit assertion period.

7) TARG drives the DB(15-0) signals to their desired pCRC values and waits at least one transmit setup time.

8) TARG negates the REQ signal and holds the DB(15-0) signals for a minimum of one transmit hold time and the P_CRCA signal asserted for a minimum of one pCRC transmit hold time.

9) TARG holds the REQ signal negated for at least one transmit REQ negation period with P_CRCA transitioning since the last REQ negation.

After either of the above sequence is complete the TARG has ended a data Group.

INIT fetches the values from the DB(15-0) signals within one receive hold time of the REQ signal. And then responds with an ACK transition.

The INIT continues to use the pad bytes, if any, for checking against the computed pCRC for the current data group. Upon receipt of the last byte of the pCRC field, the received pCRC and computed pCRC shall be compared. If they do match (i.e., no pCRC error). then the INIT negates the ACK signal.

If received pCRC and computed pCRC do not match (i.e., a pCRC error is detected), or if an improperly formatted data group is transferred, then the INIT creates an attention condition or before the last transfer of the pCRC field. When the TARG switches to a MESSAGE OUT phase the INIT sends an INITIATOR DETECTED ERROR message to the TARG. This message notifies the TARG that data contained within the data group was invalid.

If the TARG does not retry transferring the information transfer or it exhausts its retry limit the TARG goes into a STATUS phase and send a CHECK CONDITION status with a sense key set to ABORTED COMMAND and an additional sense code set to INITIATOR DETECTED ERROR MESSAGE RECEIVED for the task associated with the received INITIATOR DETECTED ERROR message.

(d) Data Group Pad field and pCRC field transfer from INIT to TARG

If the I/O signal is false (transfer to the target), the INIT determines the data field transfer is complete by detecting an assertion of the P_CRCA signal. If the REQ signal is asserted (i.e., pad field required) the INIT shall first transfer the two pad bytes, then the four pCRC bytes. If the REQ signal is negated (i.e., no pad field required) the INIT shall transfer the four pCRC bytes.

Pad field data and pCRC field data are transferred using the same negotiated values as the data field data.

The TARG may continue to send REQs, up to the negotiated offset, for the next data group. The TARG shall not transition REQ with P_CRCA asserted until the initiator has responded with all ACK transitions for the previous data group.

When the INIT detects an assertion of the P_CRCA signal and the REQ signal is asserted (i.e., pad field required), the transmission sequence is the following way.

1) Transfer data bytes for all outstanding REQs received prior to the REQ that had the P_CRCA signal asserted. INIT drives the DB(15-0) signals to their desired pad values.

2) INIT delays at least one transmit setup time, negates the ACK signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the ACK signal negated for a minimum of a transmit assertion period.

3) INIT drives the DB(15-0) signals to their desired pCRC values, delays at least one transmit setup time, asserts the ACK signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the ACK signal asserted for a minimum of a transmit assertion period.

4) INIT drives the DB(15-0) signals to their desired pCRC values and delays at least one transmit setup time.

5) INIT negates the ACK signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the ACK signal negated for a minimum of a transmit assertion period.

When the INIT detects an assertion of the P_CRCA signal and the REQ signal is negated (i.e., no pad field required),

1) INIT transfers data bytes for all outstanding REQs received prior to the REQ that had the P_CRCA signal asserted. INIT drives the DB(15-0) signals to their desired pCRC values.

2) INIT delays at least one transmit setup time, asserts the ACK signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the ACK signal asserted for a minimum of a transmit assertion period.

3) INIT drives the DB(15-0) signals to their desired pCRC values and delays at least one transmit setup time.

4) INIT negates the ACK signal and holds the DB(15-0) signals valid for a minimum of one transmit hold time and the ACK signal negated for a minimum of a transmit assertion period.

After either of the above sequence is complete the TARG has ended a data group.

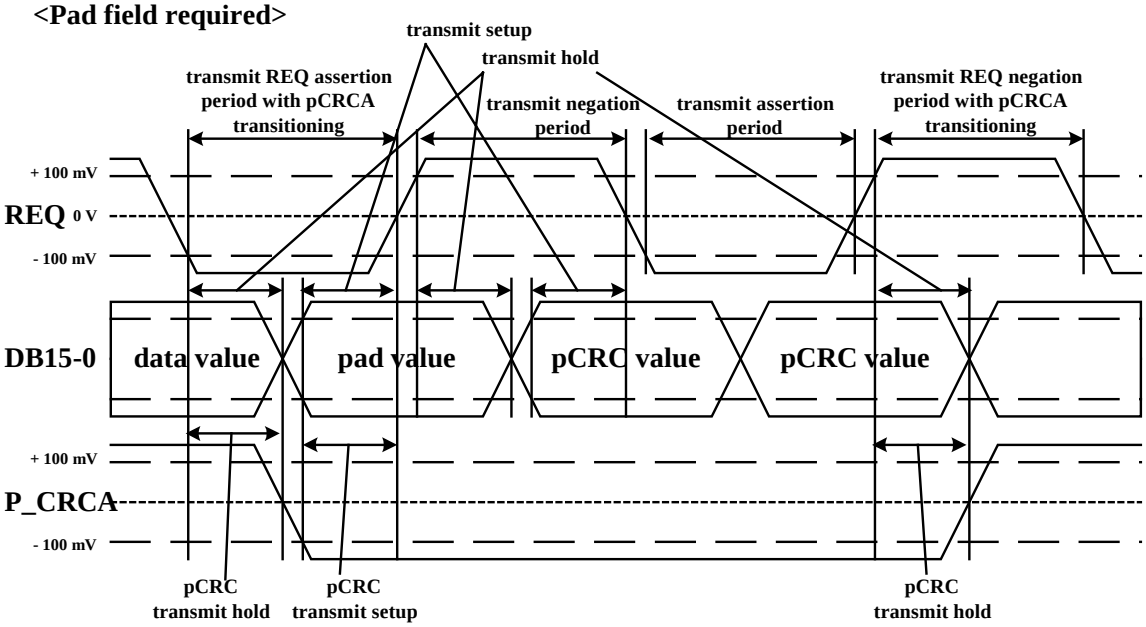
As a result of a data group always being an even number of transfers, the REQ and ACK signals are negated both before and after the transmission of the data group. The TARG fetches the value of the DB(15-0) signals within one receive hold time of the transition of the ACK signal.

The INIT uses the pad bytes, if any, in the generation of the transmitted pCRC. The TARG then uses those pad bytes, if any, for checking against the computed pCRC for the current data group. Upon receipt of the last byte of the pCRC field, the received pCRC and computed pCRC is compared.

If received pCRC and computed pCRC do not match (i.e., a pCRC error is detected), or if an improperly formatted data group is transferred, then the associated data group is considered invalid.

If the TARG does not retry transferring the information transfer or it exhausts its retry limit the TARG goes into a STATUS phase and send a CHECK CONDITION status with a sense key set to ABORTED COMMAND and an additional sense code set to SCSI PARITY ERROR for the task associated with the pCRC error.

<Pad field required>



<Pad field no required>

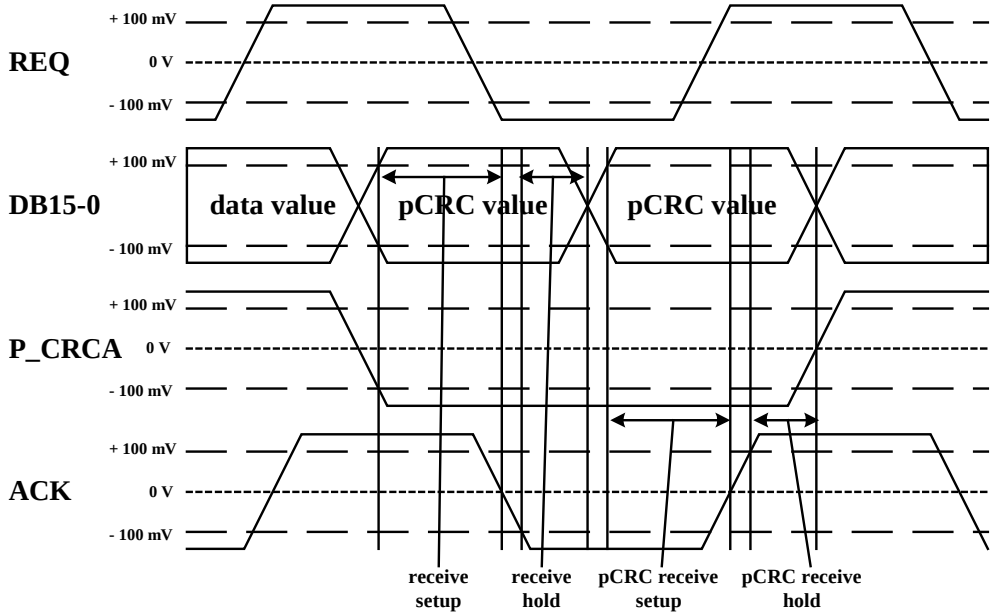


Figure 1.33 Data Group Pad field and pCRC field transfer

1.6.5.3 Paced transfer

(1) Paced transfer overview

If a paced transfer agreement has been established it shall be used in DT DATA phase and information unit transfers shall be used. The transfer agreement also specifies the REQ/ACK offset and the transfer period.

When paced transfers are being used data shall be transferred using DT data transfers on 16-bit wide buses that transmit and receive data using LVD transceivers.

If driver precompensation is enabled at the SCSI device, that SCSI device shall apply driver precompensation to all the data, parity, REQ, and ACK signals.

During paced DT data transfers, if the phase of the P1 signal indicates data is valid (see 1.6.5.3.3) on REQ or ACK assertions, data shall be clocked by the originating SCSI device by both the assertion and negation of the REQ or ACK signal lines. The receiving SCSI device shall clock DT data on both the assertion and negation of the REQ or ACK signal line after having been processed by the receiving SCSI device. If the phase of the P1 signal indicates data is invalid on REQ or ACK assertions, data shall not be clocked by the originating SCSI device and shall be ignored by the receiving SCSI device. If driver precompensation is enabled at the originating SCSI device, the originating SCSI device shall apply driver precompensation to all the data signals, the P_CRCA signal, the P1 signal, and the REQ, and or ACK signal. For paced DT DATA IN phases the REQ/ACK offset specifies the maximum number of data valid state REQ assertions that shall be sent by the TARG in advance of the number of ACK assertions received from the INIT. If the number of data valid state REQ assertions exceeds the number of ACK assertions by the REQ/ACK offset, the TARG will change P1 to enable the data invalid state prior to the next assertion of REQ and will not change P1 to enable a data valid state until after the next ACK assertion is received. For successful completion of a paced DT DATA IN phase the number of data valid state REQ assertions and ACK assertions shall be equal. Each assertion indicates a single 32-bit data transfer.

For paced DT DATA OUT phases the REQ/ACK offset specifies the maximum number of REQ assertions that will be sent by the TARG in advance of the number of data valid state ACK assertions received from the INIT. If the number of REQ assertions exceeds the number of data valid state ACK assertions by the REQ/ACK offset, the TARG will not assert REQ until after the next data valid state ACK assertion is received. For successful completion of a paced DT DATA OUT phase the number of REQ assertions and data valid state ACK assertions shall be equal. Each assertion indicates a single 32-bit data transfer. Implementors shall not use the following subclauses for timing requirements.

(2) Paced transfer training pattern

If retain training information is disabled a training pattern shall be transferred at the start of the first DT data phase for each data transfer direction after each physical connect and physical reconnect. The training pattern shall not be transferred again until after a physical disconnection occurs.

If the retain training information is enabled a training pattern shall be transferred at the start of the first DT data phase for each data transfer direction after the retain training information is enabled. The SCSI device shall save training configuration values for each I_T nexus that has negotiated to retain training information. The SCSI device shall use the saved training configuration values for all paced transfers. The TARG retrains an I_T nexus if it determines the training configuration values are invalid, without having to renegotiate the retain training information protocol option.

If the retain training information is enabled and a port changes from a INIT to a TARG that TARG shall retrain if the saved training configuration values were saved while the port was a INIT.

The receiving SCSI device shall use some or all elements of the training pattern to achieve deskewing. The transmitting SCSI device shall not make an intentional shift in relative timing between the data bus signals and the REQ or ACK signal during the DT data phase.

Note :

The requirement to not intentionally change relative timing does not include the effects of ISI, noise, or jitter.

The training pattern consists of three sections; A, B, and C. Each section contains a different pattern that may be used to train circuits within a receiver.

(a) DT DATA IN phase training pattern

The TARG indicates a training pattern is going to occur on a DT DATA IN phase by:

1) Releasing SEL for a minimum of two system deskew delays;
2) asserting the SEL signal a minimum of two system deskew delays; and
3) then asserting the REQ signal.

The TARG begins the section A of its training sequence by transmitting the following training pattern:

Start of section A:

1) if precompensation is enabled then set the drivers to the strong driver state;

2) simultaneously assert REQ, P1, P_CRCA, and DB(15-0) signals;

3) wait the equivalent of 32 transfer periods (e.g., 200 ns at fast-160);

4) simultaneously negate REQ, P1, P_CRCA, and DB(15-0) signals;

5) wait the equivalent of 32 transfer periods;

6) set precompensation to negotiated state;

7) negate SEL signal;

8) simultaneously assert and negate REQ, P1, P_CRCA, and DB(15-0) signals at the negotiated transfer period 64 times, (e.g., (2 x 6,25 ns) x 64 = 800 ns at fast-160);

Start of section B:

1) wait the equivalent of 192 transfer periods from the first assertion of REQ in step 2 of section A (e.g., 1200 ns at fast-160);

2) keep the P1, P_CRCA, and DB(15-0) signals negated while continuing to assert and negate REQ at the negotiated transfer period for the equivalent of 8 transfer periods (e.g., 50 ns at fast-160);

3) keep the P1, P_CRCA, DB(15-0), and REQ signals negated for the equivalent of 8 additional transfer periods;

4) simultaneously assert and negate P1, P_CRCA, and DB(15-0) signals at twice the negotiated transfer period (i.e., simultaneously repeat a 1100b bit pattern 12 times on each signal) while asserting and negating REQ at the negotiated transfer period 24 times (e.g., (2 x 6,25 ns) x 24 = 300 ns at fast-160);

Start of section C:

5) assert and negate REQ at the negotiated transfer period 64 times and at the same time assert and negate P1 at twice the negotiated transfer period while repeating a 0000010011111011b bit pattern eight times on each of the P_CRCA and DB(15-0) signals (e.g., (2 x 6,25 ns) x 64 = 800 ns at fast-160); and

The INIT shall begin its training pattern independent of the start of the TARGs training pattern if it detects the SEL, MSG, and I/O true and C/D false on the first assertion of the REQ signal. The INIT shall transmit the following training pattern:

1) assert ACK signal within 200 ns of the first REQ assertion;

2) if precompensation is enabled then set the drivers to the strong driver state;

3) wait the equivalent of 32 transfer periods (e.g., 200 ns at fast-160);

4) negate ACK signal;

5) wait the equivalent of 32 transfer periods (e.g., 200 ns at fast-160);

6) set precompensation to negotiated state; and

7) assert and negate ACK signal at the negotiated transfer period 32 times, (e.g., (2 x 6,25) x 32 = 400 ns at fast-160).

At the completion of its training pattern the TARG continues asserting and negating the REQ signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12,5 ns transfer period at fast-160). When the TARG is ready to transfer data it shall reverse the phase of P1.

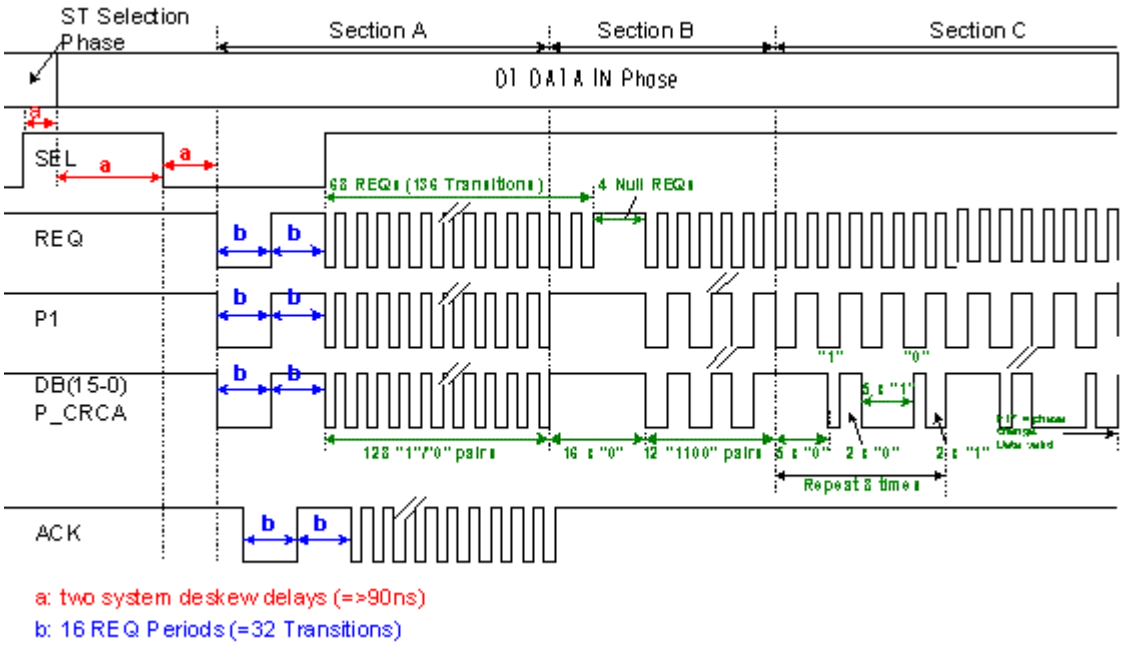


Figure 1.34 DT DATA IN phase training pattern

(b) DT DATA OUT phase training pattern

The TARG requests a training pattern on a DT DATA OUT phase by asserting the SEL signal a minimum of two system deskew delays before asserting the REQ signal. The TARG begins its training sequence by transmitting the following training pattern:

1) if precompensation is enabled then set the drivers to the strong driver state;

2) simultaneously assert REQ and P_CRCA signals;

3) wait the equivalent of 32 transfer periods (e.g., 200 ns at fast-160);

4) simultaneously negate REQ and P_CRCA signals;

5) wait 32 the equivalent of transfer periods (e.g., 200 ns at fast-160);

6) set precompensation to negotiated state;

7) negate SEL signal;

8) simultaneously assert and negate REQ and P_CRCA signals at the negotiated transfer period 32 times, (e.g., (2 x 6,25) x 32 = 400 ns at fast-160);

9) negate REQ and P_CRCA for at least the equivalent of 16 transfer periods (e.g., 100 ns at fast-160); and

10) the TARG shall begin asserting and negating REQ to indicate to the INIT valid data may be sent. The number of REQ assertions shall not exceed the negotiated REQ/ACK offset.

The INIT shall begin the section A of its training pattern independent of the start of the TARGs training pattern if it detects the SEL and MSG true, and C/D and I/O false on the first assertion of the REQ signal. The INIT shall transmit the following training pattern:

Start of section A:

1) if precompensation is enabled then set the drivers to the strong driver state;

2) simultaneously assert ACK, P1, and DB(15-0) signals within the equivalent of 32 transfer periods of the first REQ assertion (e.g., 200 ns at fast-160);

3) wait the equivalent of 32 transfer periods (e.g., 200 ns at fast-160);

4) simultaneously negate ACK, P1, and DB(15-0) signals;

5) wait the equivalent of 32 transfer periods;

6) set precompensation to negotiated state;

7) simultaneously assert and negate ACK, P1, and DB(15-0) signals at the negotiated transfer period 64 times, (e.g., (2 x 6,25) x 64 = 800 ns at fast-160);

Start of section B:

1) wait the equivalent of 192 transfer periods from the first assertion of ACK in step 2 of section A (e.g., 1200 ns at fast-160);

2) keep the P1, and DB(15-0) signals negated while continuing to assert and negate ACK at the negotiated transfer period for the equivalent of 8 transfer periods (e.g., 50 ns at fast-160);

3) keep the P1, DB(15-0), and ACK signals negated for the equivalent of 8 additional transfer periods;

4) simultaneously assert and negate P1 and DB(15-0) signals at twice the negotiated transfer period (i.e., simultaneously repeat a 1100b bit pattern 12 times on each signal) while asserting and negating ACK at the negotiated transfer period 24 times (e.g., (2 x 6,25 ns) x 24 = 300 ns at fast-160); and

Start of section C:

5) assert and negate ACK at the negotiated transfer period 64 times and at the same time assert and negat e P1 at t wi ce t he negot i at ed t r ansf er peri od whi l e r epeat i ng a 0000010011111011b bit pattern eight times on each of the DB(15-0) signals (e.g., (2 x 6,25 ns) x 64 = 800 ns at fast-160).

At the completion of its training pattern the INIT continues asserting and negating the ACK signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12,5 ns transfer period at fast-160). When the INIT is ready to transfer data and the REQ/ACK offset value is not zero it shall reverse the phase of P1.

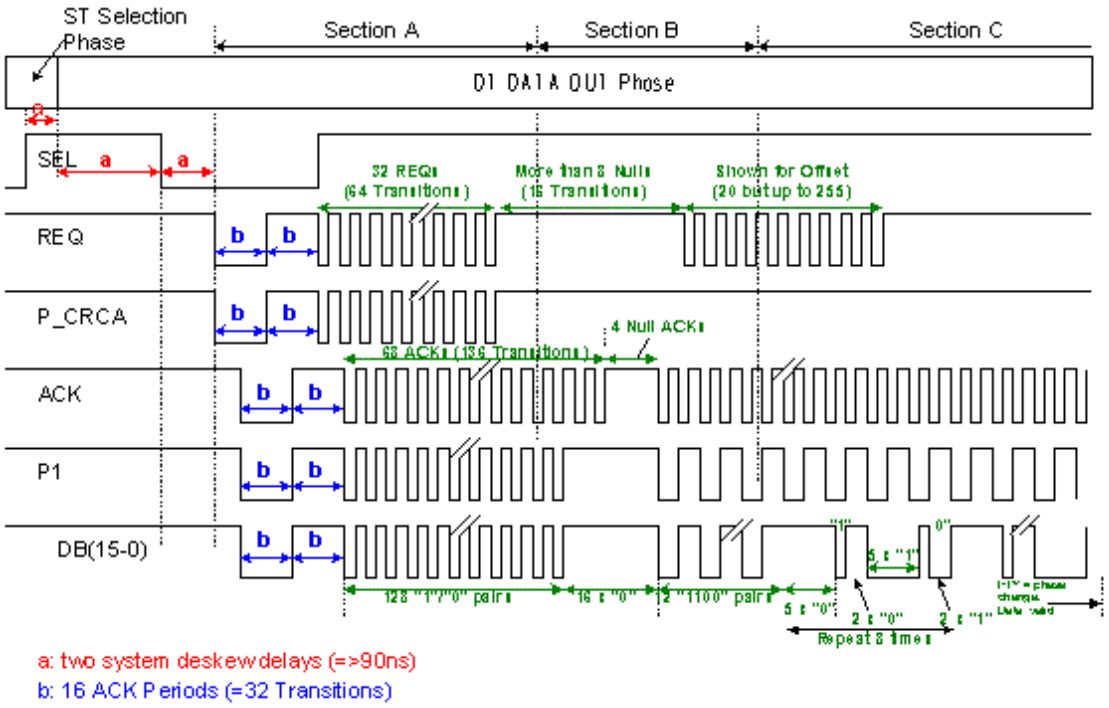


Figure 1.35 DT DATA OUT phase training pattern

(3) P1 data valid/invalid state transitions

The transmitting SCSI device port shall indicate the start of a data valid state by reversing the phase of the P1 signal coincident with a REQ or ACK assertion. This is accomplished by withholding the next transition of P1 at the start of the first two transfer periods of valid data. Beginning with the third valid data word, P1 shall be toggled every two transfer periods, coincident with a REQ or ACK assertion. The minimum duration of the data valid state is two transfer periods, and the data valid state shall consist of an even number of transfer periods. Anytime the sending SCSI device port pauses the sending of data, it shall reverse the phase of P1 by withholding the next transition of P1 at the start of the first two transfer periods that have invalid data.

Beginning with the third transfer period with invalid data, P1 shall be toggled every two transfer periods until valid data is sent. The data invalid state shall have at least one transition of P1 before changing states. The minimum data invalid time is four transfer periods. This ensures a maximum run length of three cycles for P1. The data invalid state shall last an even number of transfer periods.

From the data invalid state, the sending SCSI device port may resume sending data by reversing the phase of P1 again.

P1 has the same transmit setup and hold time requirements as data and shall always be detected by the receiving device on the assertion edge of the delayed clocked REQ or ACK signal.

See Figure.1.36 for examples of how the P1 signal is used to determine when the REQ or ACK transition clocks valid data.

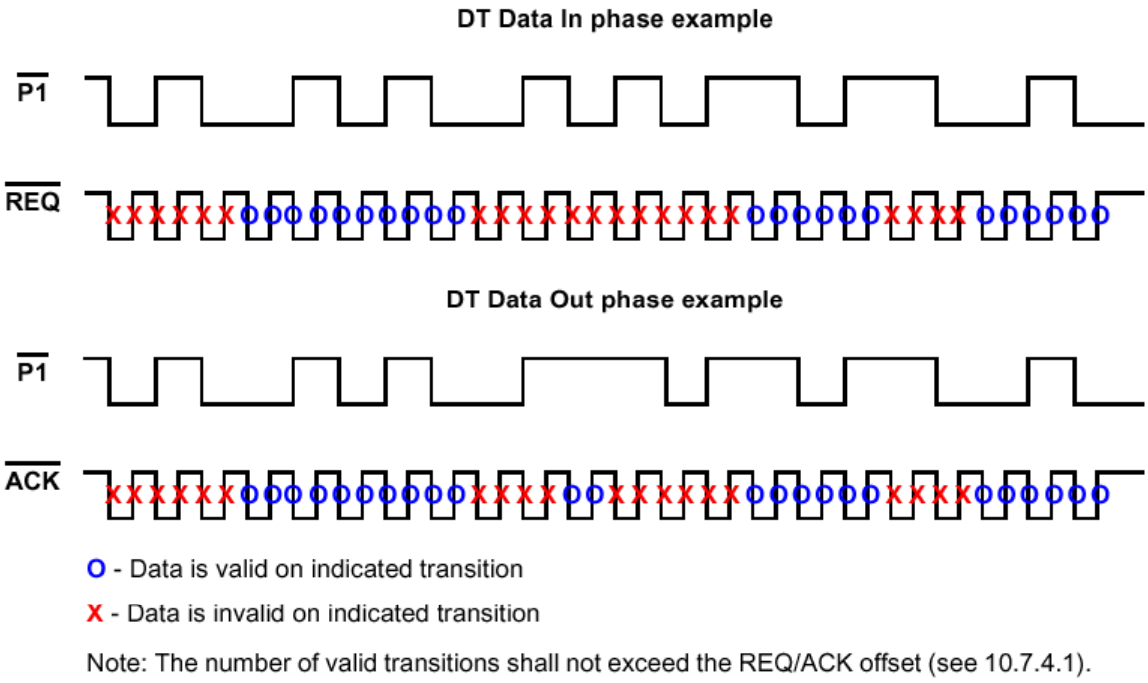


Figure 1.36 Usage of P1 to establish data valid and data invalid states

(a) Starting pacing transfers at end of training pattern

See (2) Paced transfer training pattern for the description of starting a data valid state after a training pattern.

(b) Starting pacing transfers with no training pattern

Before starting the DT DATA IN phase the TARG will wait at least two system deskew delays after the SEL signal is negated before the first assertion of the REQ signal.

The DT DATA IN phase without training starts on the first assertion of REQ if the SEL is not asserted.

The TARG begins pacing transfers only after meeting all the following:

a) signal restrictions between information transfer phases;

b) the signal restrictions between a RESELECTION phase and a DT DATA IN phase;or

c) the signal restrictions between a SELECTION phase and a DT DATA OUT phase.

The TARG begins pacing transfers by:

1) simultaneously with the assertion of REQ the TARG shall begin asserting and negating P1 at twice the negotiated transfer period (e.g., 12,5 ns for fast-160);

2) TARG asserts and negates P1 at least 8 times (e.g., (2 x 6,25 ns) x 8 = 100 ns at fast-160); and

3) the TARG may establish a data valid state by changing the phase of P1.

The DT DATA OUT phase without training starts on the first assertion of REQ if the SEL is not asserted.

The TARG begins pacing transfers only after meeting all the following:

a) signal restrictions between information transfer phases;

b) the signal restrictions between a RESELECTION phase and a DT DATA IN phase; or

c) the signal restrictions between a SELECTION phase and a DT DATA OUT phase.

The INIT shall begin pacing transfers by:

1) simultaneously with the assertion of ACK the INIT shall begin asserting and negating P1 at twice the negotiated transfer period (e.g., 12,5 ns for fast-160);

2) INIT shall assert and negate P1 at least 8 times (e.g., (2 x 6,25 ns) x 8 = 100 ns at fast-160); and

3) the INIT may establish a data valid state by changing the phase of P1.

(c) Ending pacing transfers

After transmitting the last data word of a DT DATA IN phase the TARG ends pacing by waiting for all REQs to be responded to by ACKs then negate the REQ and P1 signals. After the TARG stops asserting and negating REQ it will not assert REQ again until the requirements in 10.12 are met.

After transmitting the last data word of a DT DATA OUT phase the INIT shall;

a) continue asserting and negating the ACK and P1 signals until it detects a change to the C/D, I/O, or MSG signals; and

b) negate the ACK and P1 signals within 200 ns of detecting a change to the C/D, I/O, or MSG signals;

When the TARG changes from a DT DATA OUT phase to any other phase it will wait at least a bus settle delay plus a data release delay before asserting REQ and ignore any ACK transitions for at least a bus settle delay plus a data release delay after transitioning the C/D, I/O, or MSG signals.

(4) Paced information unit transfer

Information units shall be transferred on the DT DATA OUT phase and the DT DATA IN phase, and the information units' embedded iuCRC shall be used to detect information unit data errors. If the I/O signal is true (i.e., transfer to the INIT) and the phase of the P1 signal indicates data is valid, to transfer SPI information units the TARG:

1) drives the DB(15-0) signals to their values simultaneous with the next REQ signal assertion;

2) holds the DB(15-0) signals valid for a minimum of one transmit hold time;

3) drives the DB(15-0) signals to their values simultaneous with the next REQ signal negation; and

4) holds the DB(15-0) signals valid for a minimum of one transmit hold time.

If the I/O signal is true (i.e., transfer to the INIT), to receive SPI information units the INIT shall:

1) Read the value on the DB(15-0) signals within one receive hold time of the transition of the REQ signal; and

2) respond with an ACK signal assertion after each REQ assertion/negation pair.

If the I/O signal is false (i.e., transfer to the TARG) and the phase of the P1 signal indicates data is valid, to transfer SPI information units the INIT:

1) Shall wait until detecting a REQ assertion;

2) shall drive the DB(15-0) signals to their values simultaneous with the next ACK signal assertion;

3) shall hold the DB(15-0) signals valid for a minimum of one transmit hold time;

4) shall drive the DB(15-0) signals to their values simultaneous with the next ACK signal negation; and

5) shall hold the DB(15-0) signals valid for a minimum of one transmit hold time.

If the I/O signal is false (i.e., transfer to the TARG), to receive SPI information units the TARG:

1) reads the value of the DB(15-0) signals within one receive hold time of the transition of the ACK signal.

If write flow control is enabled and the current SPI data stream information unit is the last SPI data stream information unit of the stream then:

1) The TARG asserts the P_CRCA signal a minimum of a flow control transmit setup time before the end of the last information unit and shall keep the P_CRCA signal asserted for a flow control transmit hold time;

2) The TARG does not assert the P_CRCA signal until a minimum of a flow control hold time after the end of the previous information unit; and

3) The TARG negates the P_CRCA signal a minimum of a flow control transmit setup time before the start of the next information unit.

Note :

The earlier in a SPI data stream information unit that the TARG asserts the P_CRCA signal, the better the INIT may manage data pre-fetch.

As a result of a SPI information unit always being an even number of transfers, the REQ and ACK signals are negated both before and after the transmission of the SPI information unit.

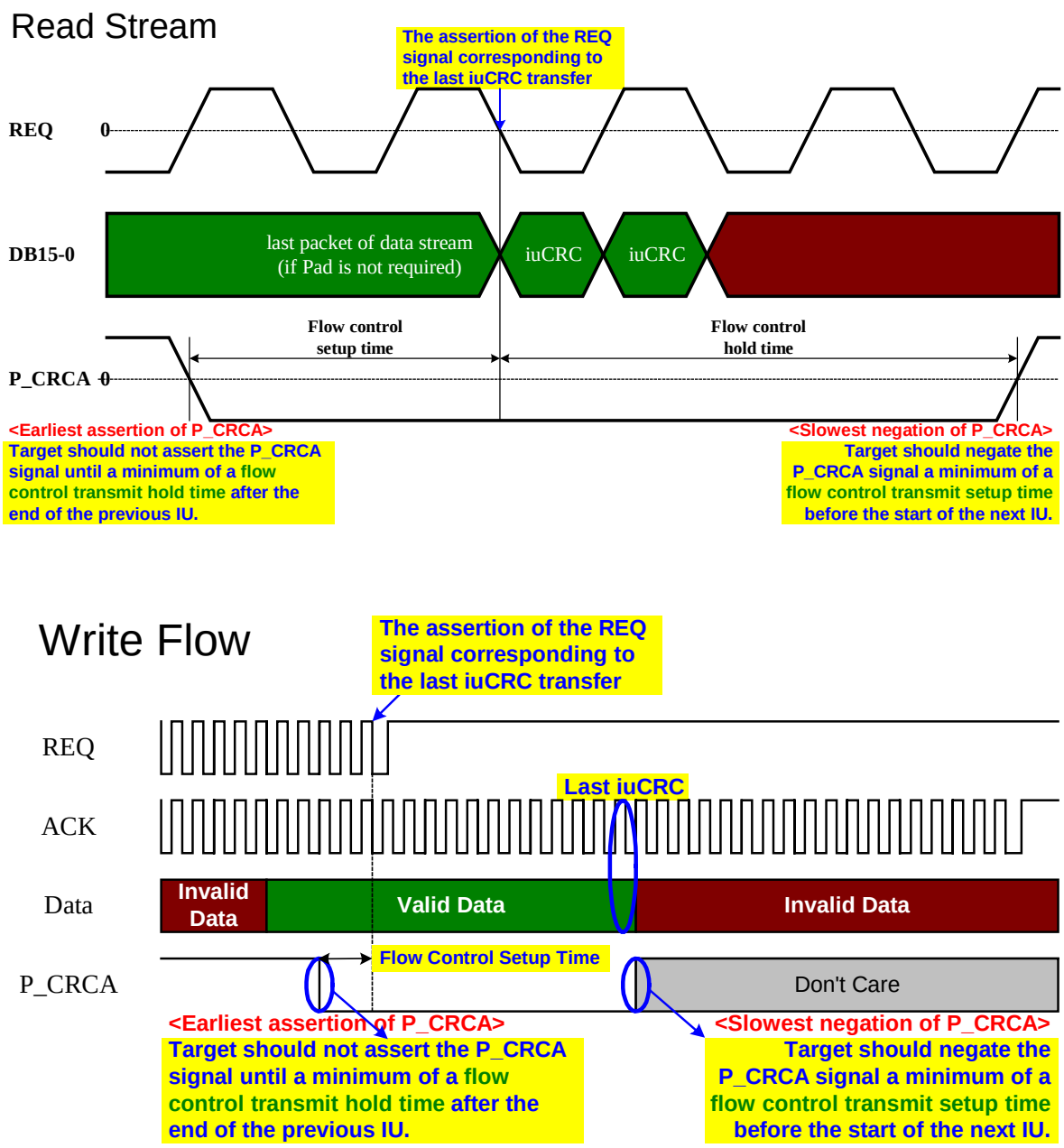


Figure 1.37 READ STREAM and WRITE FLOW

(5) Deskewing

The deskewing is a technique to compensate incoming Data and REQ/ACK signal skew. The deskewing is done during training sequence, and it adjust the timing of P1, P_CRCA and DB(15-0) to be optimum against REQ/ACK. The deskewing is only enabled in paced transfers.

(6) DT DATA phase information unit transfer exception condition handling

When information unit transfers are enabled (see Section 1.9):

(a) DT DATA IN phase

The INIT shall not negate the ACK for the last byte of the last iuCRC in an information unit until the entire information unit has been verified and any required attention condition has been established.

If the nexus has been fully identified (i.e., an I_T_L_Q nexus has been established) and the INIT detects an iuCRC error in any information unit it receives, other than a SPI status information unit, then the SCSI initiator port shall create an attention condition on or before acknowledging the last iuCRC of the failed information unit. When the TARG switches to a MESSAGE OUT phase the INIT shall send an INITIATOR DETECTED ERROR message (see 2.3.5) to the TARG. This message notifies the TARG that data in the information unit was invalid.

If the INIT detects an iuCRC error in a SPI status information unit, the INIT shall create an attention condition on or before the last iuCRC of the information unit is acknowledged. If the TARG detects an attention condition, it shall switch to a MESSAGE OUT phase and the INIT shall send an INITIATOR DETECTED ERROR message (see 2.3.5) or an ABORT TASK message to the TARG. These messages notify the TARG that the SPI status information unit was invalid.

If a nexus has been fully identified and the information unit that failed was not a SPI status information unit and the message received from the INIT was an INITIATOR DETECTED ERROR message then the TARG shall send a SPI L_Q/SPI status information unit pair to the INIT with a CHECK CONDITION status and a sense key set to ABORTED COMMAND and an additional sense code set to INITIATOR DETECTED ERROR MESSAGE RECEIVED for the task associated with the received INITIATOR DETECTED ERROR message.

If the information unit that failed was a SPI status information unit and the message received was an INITIATOR DETECTED ERROR message, then the TARG shall retry transferring the SPI L_Q/SPI status information unit pair to the INIT with the original status information.

If the information unit that failed was a SPI status information unit and the message received was an ABORT TASK message then the TARG shall cause a bus free by generating a BUS FREE phase.

If the INIT is receiving a SPI L_Q information unit and the INIT detects an iuCRC error (i.e., the nexus identification fails) while in the DT DATA IN phase the INIT shall create the attention condition on or before the acknowledgment of the last iuCRC. When the TARG switches to a MESSAGE OUT phase the INIT shall send an INITIATOR DETECTED ERROR message (see 2.3.5) to the TARG. This message notifies the TARG that the nexus identification failed. The TARG shall then cause a bus free by generating a BUS FREE phase. The TARG shall retry the task associated with the failed SPI L_Q information unit.

If the INIT receives a SPI L_Q information unit with a type code that is not defined in Table 1.25 that INIT shall create an attention condition on or before the acknowledgment of the last iuCRC. When the TARG switches to a MESSAGE OUT phase the INIT shall send an ABORT TASK message (see 2.3.12) to the TARG. The message notifies the TARG that the SPI L_Q information units type code was rejected. The TARG shall then cause a bus free by generating a BUS FREE phase.

(b) DT DATA OUT phase

The TARG shall only respond to an iuCRC error after all the data in an information unit has been received.

If the nexus has been fully identified (i.e., an I_T_L_Q nexus has been established) and the TARG detects an iuCRC error in any SPI data information unit, SPI data stream information unit, or last command SPI command information unit it receives while in the DT DATA OUT phase the TARG shall switch to a DT DATA IN phase and send a SPI L_Q/SPI status information unit pair to the INIT, before sending any other SPI L_Q information unit. The status information shall indicate a CHECK CONDITION status and a sense key set to ABORTED COMMAND and the additional sense code set to INFORMATION UNIT iuCRC ERROR DETECTED for the task associated with the iuCRC error.

If the TARG detects an iuCRC error on an iuCRC interval that is not at the end of a SPI information unit the TARG shall not respond to the error until all the bytes of the SPI information unit in which the error occurred have been transferred. The TARG may discard the transmitted information.

If the TARG is receiving a SPI L_Q information unit and the TARG detects an iuCRC error (i.e., the nexus identification fails) the TARG shall cause an unexpected bus free by generating a BUS FREE phase (see 10.3).

If a TARG receives a SPI L_Q information unit with a type code that is not defined in Table 1.25 that TARG shall transfer all the bytes indicated in the DATA LENGTH field and iuCRC INTERVAL field and shall discard the transmitted information for the information unit that follows the SPI L_Q information unit. After transferring all the bytes the TARG shall change to a DT DATA IN phase and transmit a SPI status information unit with a RSPVALID bit of one and the packetized failure code set to INVALID TYPE CODE RECEIVED IN SPI L_Q INFORMATION UNIT.

If a TARG receives a SPI L_Q information unit with an illegal data length the TARG shall transfer all the bytes indicated by the data length and iuCRC interval and shall discard the transmitted information. After transferring all the bytes the TARG shall change to a DT DATA IN phase and transmit a SPI status information unit with a RSPVALID bit of one and the packetized failure code set to ILLEGAL REQUEST RECEIVED IN SPI L_Q INFORMATION UNIT.

1.6.5.4 Wide mode transfer (16-bit SCSI)

The wide mode transfer enables information transfer using a multiple-byte-wide data bus. It is used only in DATA phases.

In wide mode transfer, the WIDE DATA TRANSFER REQUEST or PARALLEL PROTOCOL REQUEST message should first be exchanged by the INIT and the TARG to define the data transfer mode between SCSI devices. When the WIDE DATA TRANSFER REQUEST or PARALLEL PROTOCOL REQUEST message is exchanged, a data bus width is determined. Figure 1.38 shows the data sequence at data transfer. When a wide data transfer agreement is negotiated in PARALLEL PROTOCOL REQUEST data bus width is determined 16 bit mode automatically.

Note:

The IDD supports 8-bit and 16-bit transfer modes. The initial value of the data bus width is "8-bit mode". After power is turned on, a RESET condition occurs, or a TARGET RESET message is received, data is transferred using 8-bit mode until the mode is switched to "16-bit mode" by exchanging the WIDE DATA TRANSFER REQUEST message.

Number of information items transferred	P cable		
1	Unused	A	“8-bit mode”
2	Unused	B	
	DB15.....DB8	DB7.....DB0	
1	B	A	“16-bit mode”

Figure 1.38 Data sequence at data transfer

1.6.6 COMMAND phase

The COMMAND phase is a bus phase in which the TARG requests the INIT to transfer command information (CDB) to the TARG. The TARG keeps the C/D signal true and the I/O and MSG signals false during REQ/ACK handshaking in this phase.

1.6.7 DATA phase

The DATA phase is divided into DATA IN and DATA OUT phases according to the direction of data transfer. In a DATA phase, synchronous data transfer can be performed.

(1) DT DATA IN phase

The DT DATA IN phase allows the target to request that data be sent to the initiator from the target using DT data transfers. The target shall assert the I/O and MSG signals and negate the C/D signal during the REQ/ACK handshake(s) of this phase.

(2) DT DATA OUT phase

The DT DATA OUT phase allows the target to request that data be sent from the initiator to the target using DT data transfers. The target shall assert the MSG signal and negate the C/D and I/O signals during the REQ/ACK handshake(s) of this phase.

(3) ST DATA IN phase

The ST DATA IN phase allows the target to request that data be sent to the initiator from the target using ST data transfers. The target shall assert the I/O signal and negate the C/D and MSG signals during the REQ/ACK handshake(s) of this phase.

(4) ST DATA OUT phase

The ST DATA OUT phase allows the target to request that data be sent from the initiator to the target using ST data transfers. The target shall negate the C/D, I/O, and MSG signals during the REQ/ACK handshake(s) of this phase.

(5) Data transfer rate in synchronous mode

Table 1.20 lists the synchronous transfer mode parameters valid for the IDD. The actual values are determined by exchange of SYNCHRONOUS DATA TRANSFER REQUEST or PARALLEL PROTOCOL REQUEST message between the two SCSI devices. If two or more INITs are used, different parameters may be used by each INIT. The PARALLEL PROTOCOL REQUEST message are used to negotiate a synchronous data transfer agreement, a wide data transfer agreement, and set the protocol options between two SCSI devices. Although the data transfer rate is determined by the Transfer Period parameter, an appropriate REQ/ACK Offset parameter value must be selected depending on the ACK pulse response of the INIT. The interface cable length must also be considered.

Table 1.20 Parameters used for fast synchronous data transfer mode

Parameter type	Selectable value	Transfer rate	
		8-bit mode	16-bit mode
PPR Transfer Period (6)	X'08'(6.25ns) (5)	N/A	Maximum 320.00 MB/s
	X'09'(12.5ns) (4)		Maximum 160.00 MB/s
	X'0A' (25 ns) (3)		Maximum 80.00 MB/s
	X'0B' (37.5 ns) (3)		Maximum 53.30 MB/s
	X'0C' (50 ns) (2)		Maximum 40.00 MB/s
	X'11' (75 ns) (2)		Maximum 26.66 MB/s
	X'19' (100 ns) (1)		Maximum 20.00 MB/s
	X'1F' (120 ns) (1)		Maximum 16.00 MB/s
	X'25' (150 ns) (1)		Maximum 13.33 MB/s
	X'2B' (175 ns) (1)		Maximum 11.42 MB/s
	X'32' (200 ns)		Maximum 10.00 MB/s
	X'38' (225 ns)		Maximum 8.88 MB/s
	X'3E' (250 ns)		Maximum 8.00 MB/s
	X'44' (275 ns)		Maximum 7.27 MB/s
	X'4B' (300 ns)		Maximum 6.66 MB/s
	X'51' (325 ns)		Maximum 6.15 MB/s
	X'57' (350 ns)		Maximum 5.71 MB/s
	X'5D' (375 ns)		Maximum 5.33 MB/s
SDTR Transfer Period (7)	X'0A' (25 ns) (3)	Maximum 40.00 MB/s	Maximum 80.00 MB/s
	X'0B' (37.5 ns) (3)	Maximum 26.60 MB/s	Maximum 53.30 MB/s
	X'0C' (50 ns) (2)	Maximum 20.00 MB/s	Maximum 40.00 MB/s
	X'11' (75 ns) (2)	Maximum 13.33 MB/s	Maximum 26.66 MB/s
	X'19' (100 ns) (1)	Maximum 10.00 MB/s	Maximum 20.00 MB/s
	X'1F' (120 ns) (1)	Maximum 8.00 MB/s	Maximum 16.00 MB/s
	X'25' (150 ns) (1)	Maximum 6.67 MB/s	Maximum 13.33 MB/s
	X'2B' (175 ns) (1)	Maximum 5.71 MB/s	Maximum 11.42 MB/s
	X'32' (200 ns)	Maximum 5.00 MB/s	Maximum 10.00 MB/s

(1) Fast synchronous data transfer mode (Fast SCSI)
(2) Ultra fast synchronous data transfer mode (Fast-20 SCSI)
(3) Ultra-2 fast synchronous data transfer mode only for LVD (Fast-40 SCSI)
(4) Ultra-160M fast synchronous data transfer mode only for LVD (Fast-80 SCSI). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.

(5) Ultra-320 fast synchronous data transfer mode only for LVD (Fast-80 SCSI). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition and information units transfer.
(6) PPR : PARALLEL PROTOCOL REQUEST
(7) SDTR : SYNCHRONOUS DATA TRANSFER REQUEST

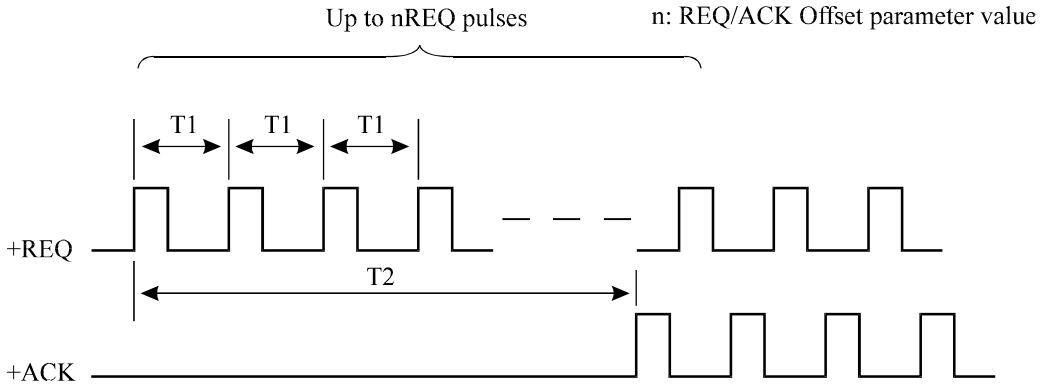


Figure 1.39 Data transfer rate in synchronous mode

1.6.8 STATUS phase

In a STATUS phase, the TARG requests to transfer status information from the TARG to the INIT. The TARG keeps the C/D and I/O signals true and the MSG signal false during REQ/ACK handshaking in this phase.

1.6.9 MESSAGE phase

The MESSAGE phase is divided into MESSAGE IN and MESSAGE OUT phases depending on the direction of message information transfer. In either phase, several messages can be transferred.

The first byte transferred in a MESSAGE phase must be a single-byte message or the first byte of a multiple-byte message. If the message consists of more than one byte, all bytes must be transferred in a single MESSAGE phase. For details of message types and their operation, refer to Chapter 2.

(1) MESSAGE IN phase

In a MESSAGE IN phase, the TARG requests to transfer message information from the TARG to the INIT. The TARG keeps the C/D, I/O, and MSG signals true during REQ/ACK handshaking in this phase.

(2) MESSAGE OUT phase

In a MESSAGE OUT phase, the TARG requests to transfer message information from the INIT to the TARG. The TARG keeps the C/D and MSG signals true and I/O signal false during REQ/ACK handshaking in this phase.

The TARG executes this phase in response to the ATTENTION condition (described in Section 1.7.1) created by the INIT, and must remain in the MESSAGE OUT phase.

Note:

The TARG can terminate the MESSAGE OUT phase even when the ATN signal is true when it returns a MESSAGE REJECT message to reject an illegal or invalid message, when it enters the BUS FREE phase as directed by the received message, or when it returns a message immediately in response to a received message (such as the SYNCHRONOUS DATA TRANSFER REQUEST).

The TARG can process a received message immediately if no parity error is detected. If a parity error is detected, the TARG shall ignore all messages which have been received after the parity error detected in the MESSAGE OUT phase.

When the TARG receives all message information correctly without detecting a parity error, the TARG shall enter the INFORMATION TRANSFER phase other than the MESSAGE OUT phase and execute at least one byte of information transfer in order to request the INIT not to retry message transfer. During some message transfer, the TARG may report the normal completion of message reception by switching to the BUS FREE phase (for example, ABORT TASK SET and TARGET RESET messages).

1.6.10 Signal requirements concerning transition between bus phases

If an SCSI bus is at an intermediate point of two INFORMATION TRANSFER phases (during transition of bus phase), the interface signals must satisfy the following requirements.

a) The BSY, SEL, and ACK signals must not change.

b) The REQ signal must not change until it is asserted to qualify the start of a new phase.

c) The C/D, I/O, MSG and DB(15-0, P_CRCA, P1) signals may change.

d) Switching the DB(15-0, P_CRCA) signals direction from OUT (INIT driving) to IN (TARG driving)

   1) The transition of the I/O signal to true.

   2) The TARG delays driving the DB(15-0, P_CRCA, and/or P1) by at least one Data Release Delay plus one Bus Settle Delay after asserting the I/O signal.

   3) The INIT releases the DB(15-0, P_CRCA, and/or P1) within one Data Release Delay

e) Switching the DB(15-0, P_CRCA and/or P1) direction from IN (TARG driving) to OUT (INIT driving)

1) The TARG negates the I/O signal.

2) The TARG releases the DB(15-0, P_CRCA and/or P1) within one System Deskew Delay.

3) The INIT detects the negation of the I/O signal.

4) The INIT asserts the DB(15-0, P_CRCA and/or P1) more than one System Deskew Delay.

f) The P_CRCA signal direction may switch direction while the DATA BUS and/or DB(P1) does not (e.g., changing from COMMAND phase to DT DATA OUT phase).

- When switching the P_CRCA signal direction from out (INIT driving) to in (TARG driving)

  1) The TARG delays driving the P_CRCA by at least one Data Release Delay plus one Bus Settle Delay after negating the C/D signal

  2) The INIT releases the P_CRCA signal within one Data Release Delay after the transition of the C/D signal to false.

- When switching the P_CRCA signal direction from in (TARG driving) to out (INIT driving)

  1) The TARG releases the P_CRCA signal within one System Deskew Delay after asserting the C/D signal.

  2) The INIT negates the P_CRCA signal more than one System Deskew Delay after the detection of the assertion of the C/D signal.

g) The ATN and RST signals may change as defined under the descriptions for the attention condition and hard reset.

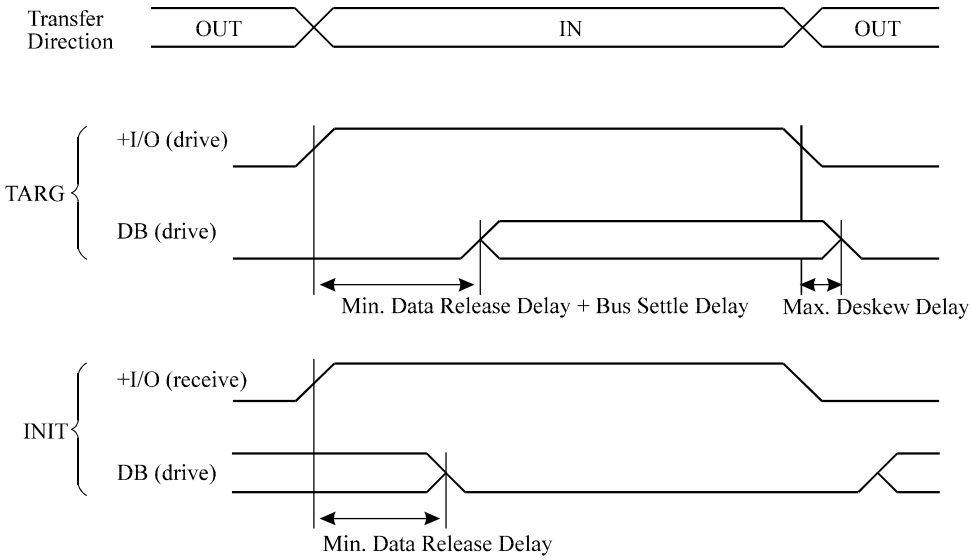


Figure 1.40 Switching direction of transfer over data bus

1.6.11 Time monitoring feature

The IDD has a time monitoring feature for the SCSI bus to prevent the hang-up of the SCSI bus in the case that the IDD cannot receive a response from the INIT in the RESELECTION phase.

The IDD monitors the response from the INIT (BSY signal) in the RESELECTION phase. When the IDD cannot receive the response within a specified period (250 ms), the IDD executes the timeout process (see Section 1.6.4) and releases the SCSI bus once. After that the IDD executes the retry process of the RESELECTION phase (see Section 3.1).

The user can select the number of retries of the RESELECTION phase by the CHANGE DEFINITION command.

Table 1.21 Retry count setting for RESELECTION phase

RSRTY bit	Retry count for RESELECTION phase
"0"	10 times
"1" (Setting at shipping)	∞ (Unlimited)

For details on setting, refer to Subsection 3.1.4, in the SCSI Logical Interface Specifications.

1.7 Bus Conditions

Two types of asynchronous control, the ATTENTION condition and RESET condition, shall be defined to control or modify the bus phase transition sequence (bus conditions).

1.7.1 ATTENTION condition

The ATTENTION condition allows the INIT to report that the INIT has a message to be sent to the TARG. The TARG receives the message from the INIT by starting the MESSAGE OUT phase. Figure 1.41 shows the ATTENTION condition.

(1) Generation and release of ATTENTION condition (INIT)

The INIT can generate the ATTENTION condition by asserting the ATN signal except for the ARBITRATION or BUS FREE phase.

When generating of an attention condition on the SELECTION phase following arbitration, the INIT must set the ATN signal true at least System Deskew Delay × 2 before releasing the BSY signal.

To create an attention condition during the SELECTION phase following a QAS, the SCSI initiator port shall assert the ATN signal at least two system deskew delays before asserting the INIT's ID on the bus.

When generating of a new ATTENTION condition in the INFORMATION TRANSFER phase, to inform the TARG of the ATTENTION condition before the transition to the next new bus phase or information unit, the INIT must set the ATN signal true before ATN transmit setup time or more from the timing of setting false the ACK signal for the last byte being transferred in the current bus phase or information unit. If the ATN sending timing is delayed, the TARG may not be informed of the ATTENTION condition until the next bus phase or information unit. The INIT may not operate as it should.

When transferring message information in several bytes in the MESSAGE OUT phase, the INIT must keep the ATN signal true. The INIT can make the ATN signal false any time except while the ACK signal is true in the MESSAGE OUT phase. When transferring the last byte in the MESSAGE OUT phase, the INIT generally makes the ATN signal false during the period between the time the REQ signal becomes true and the time it replies the ACK signal. In this case, the INIT must set the ATN signal false before Deskew Delay × 2 or more form the timing of setting true the ACK signal.

The INIT must make the ATN signal false before making the ACK signal true to transfer the last message byte if so specified for the particular type of message to the TARG. (See Subsection 2.1.2.)

(2) Response against ATTENTION condition (TARG)

The TARG shall start the MESSAGE OUT phase and respond to the ATTENTION condition in the following conditions. Also, the TARG shall enter the MESSAGE OUT phase when the ATN signal is true after the TARG returns the MESSAGE REJECT or other message with halting the MESSAGE OUT phase.

- When the ATN signal becomes true in the COMMAND phase, the TARG shall start the MESSAGE OUT phase immediately after a part or all bytes of command (CDB) has been transferred.

- When the ATN signal becomes true in the DATA phase, the TARG shall start the MESSAGE OUT phase immediately after the DATA phase. However, the TARG can enter the MESSAGE OUT phase any time when necessary. (Data transfer is not interrupted on a boundary of logical data blocks.) The INIT shall continue the REQ/ACK handshaking (in DATA phase) until the bus phase is changed.

- When the ATN signal becomes true in the STATUS phase, the TARG shall start the MESSAGE OUT phase after the end of status byte transfer

- When the ATN signal becomes true in the MESSAGE IN phase, the TARG shall start the MESSAGE OUT phase immediately after the end of current message transfer.

- When the ATN signal becomes true in the SELECTION phase, the selected TARG shall start the MESSAGE OUT phase immediately after the SELECTION phase.

- If SPI information unit transfers are disabled and an ATN signal becomes true in the RESELECTION phase, the TARG will enter MESSAGE OUT phase after the TARG has sent its IDENTIFY message for that RESELECTION phase.

- When the ATN signal becomes true in the information unit transfer, other than a SPI data stream information unit, the TARG will enter MESSAGE OUT phase at the completion of the current SPI information unit (i.e., after receiving all the ACKs from the INIT for the current SPI information unit).

- When the ATN signal becomes true in the information unit transfer, other than a SPI data stream information unit, the TARG will enter MESSAGE OUT phase at the completion of the current SPI information unit (i.e., after receiving all the ACKs from the INIT for the current SPI information unit).

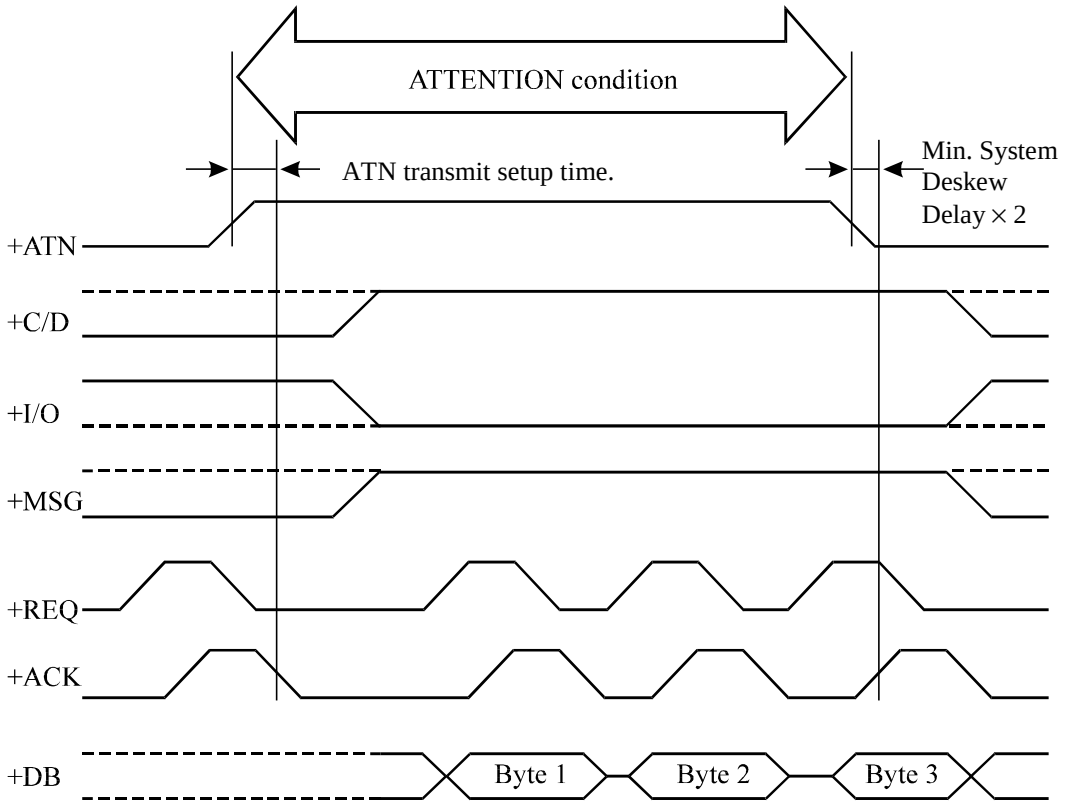
- the ATN signal becomes true between SPI information units the TARG will enter MESSAGE OUT phase at the completion of the next SPI information unit.

During a RESELECTION phase the INIT should only create an attention condition to transmit an ABORT TASK SET, ABORT TASK, TARGET RESET, CLEAR TASK SET, DISCONNECT, LOGICAL UNIT RESET, or NO OPERATION message. Other uses may result in ambiguities concerning the nexus.

In the case of more than one byte message transferred, the INIT should keep the ATN signal asserted throughout the MESSAGE OUT phase.

Unless otherwise specified, the INIT may negate the ATN signal at any time, that does not violate the specified setup and hold times, except it must not negate the ATN signal while the ACK signal is asserted during a MESSAGE OUT phase.

Normally, the INIT negates the ATN signal while the REQ signal is true and the ACK signal is false during the last REQ/ACK handshake of the MESSAGE OUT phase.



Note:

The time is specified at the SCSI connector terminal of the TARG.

Figure 1.41 ATTENTION condition

Note:

The ATTENTION condition generated by the INIT determines the message level to be used in the command execution sequence. (Details are explained in Section 2.1.3.) If the ATTENTION condition is not generated, the TARG uses a TASK COMPLETE message only.

1.7.2 RESET condition

The RESET condition allows all SCSI devices to release immediately from the bus. RESET has higher priority than any other phases and bus conditions. Any SCSI device can generate the RESET condition anytime by keeping the RST signal true for Reset Hold Time or more. The state of all bus signals except RST signals are undefined during the RESET condition.

All SCSI devices shall stop driving all bus signals (except for the RST signal) and release the bus within Bus Clear Delay after the RST signal becomes true. After the RESET condition, the SCSI bus always enters the BUS FREE phase. Figure 1.42 shows the RESET condition.

The following are the IDD operations when the RESET condition is detected.

1) Clears all commands including the currently executing commands and queued commands.

2) Releases the reserved disk state of the disk drive.

3) Initializes the operation mode to its initial status just after power-on if it has been set by the message or command.

   - The current value of the parameter set by the MODE SELECT command is initialized to the saved value previously established. If the value is not saved, it is initialized to the default value.
   - The synchronous transfer parameters defined between the IDD and other SCSI device are cleared. Any data transfer mode between all SCSI devices is initialized to the asynchronous mode.

4) The UNIT ATTENTION condition is generated for all SCSI devices.

5) The sense data is no longer retained and is cleared.

6) All data read into the data buffer in advance by the read-ahead cache feature is invalidated.

Notes:

1. The IDD does not generate a RESET condition.

2. The IDD provides only "hard" RESET condition specified by the SCSI standard.

3. Reset Hold Time is specified to guarantee that any SCSI device can recognize the occurrence the RESET condition. On the IDD, even if the pulse width is less than Reset Hold Time, the RESET condition is effective.

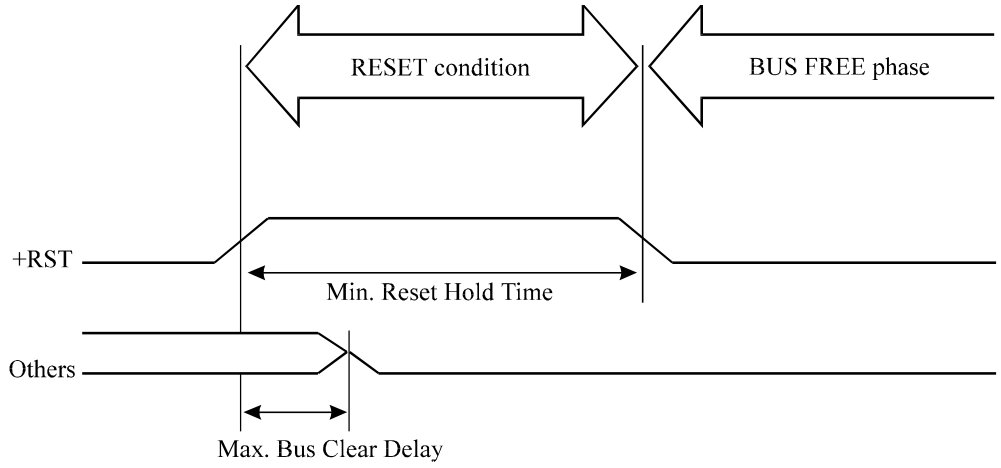


Figure 1.42 condition

1.8 Bus Phase Sequence

1.8.1 Bus Phase Sequence with Information Units Disabled

The SCSI bus phases are switched in the specific sequence depending on the command execution by the TARG. When the TARG asserts the BSY signal true in the SELECTION or RESELECTION phase, the status change of SCSI bus is controlled by the TARG except for the ATTENTION and RESET conditions.

The RESET condition can stop all bus phases and force the SCSI bus to switch to the BUS FREE phase. Also, it can switch the bus from any phase to the BUS FREE phase.

Note:

The TARG can enter the BUS FREE phase in order to report an error condition. For details, see Section 1.6.1.

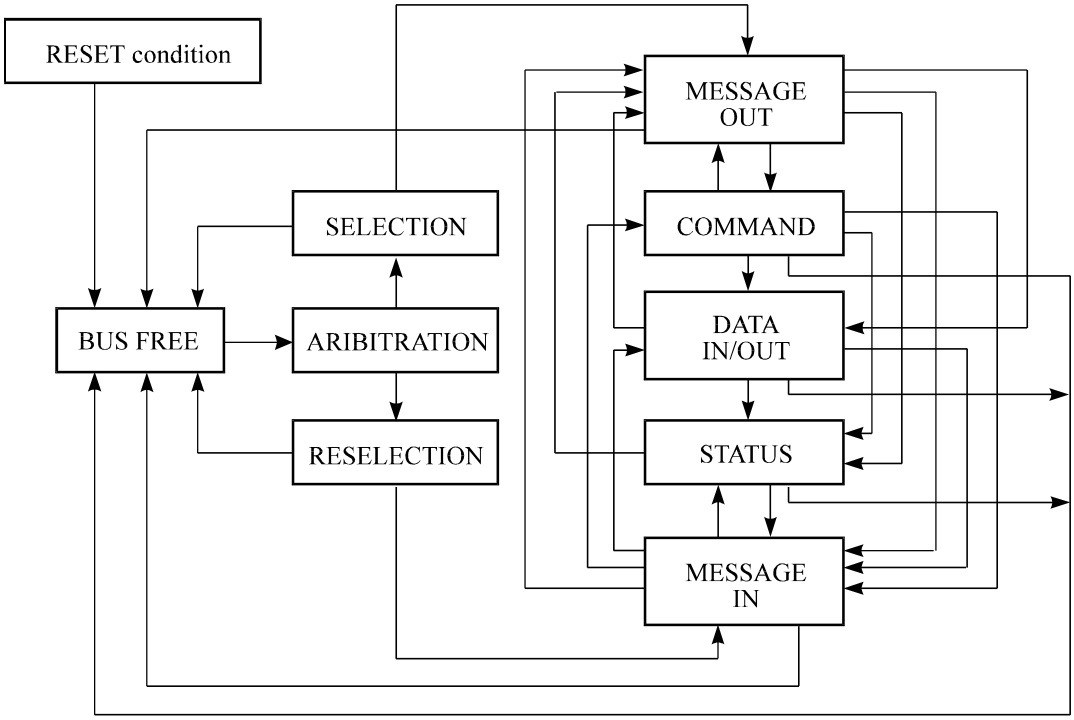
Figure 1.43 shows the allowable bus phase sequence. Figure 1.44 provides an example of bus phase sequence during single command execution.

Note:

Figure 1.43 shows the bus phase sequence applied to the system which uses the ARBITRATION phase and the system which does not use the phase. Also, this Figure compares the operations when the MESSAGE OUT phase is used and when it is not used.

The use of MESSAGE OUT phase is determined by the generation of ATTENTION condition by the INIT. If the ATTENTION condition is not generated, the TARG assumes that the INIT does not support any message other than the TASK COMPLETE and the TARG uses only the TASK COMPLETE message in the subsequent command sequence.

[When ARBITRATION is used with MESSAGE OUT]



[When ARBITRATION is used without MESSAGE OUT]

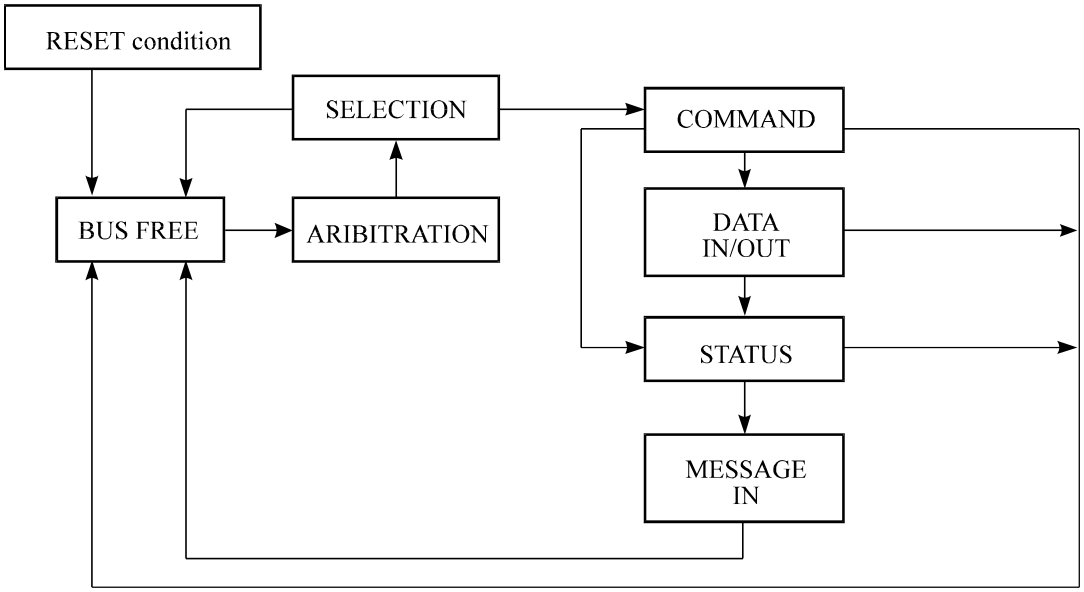
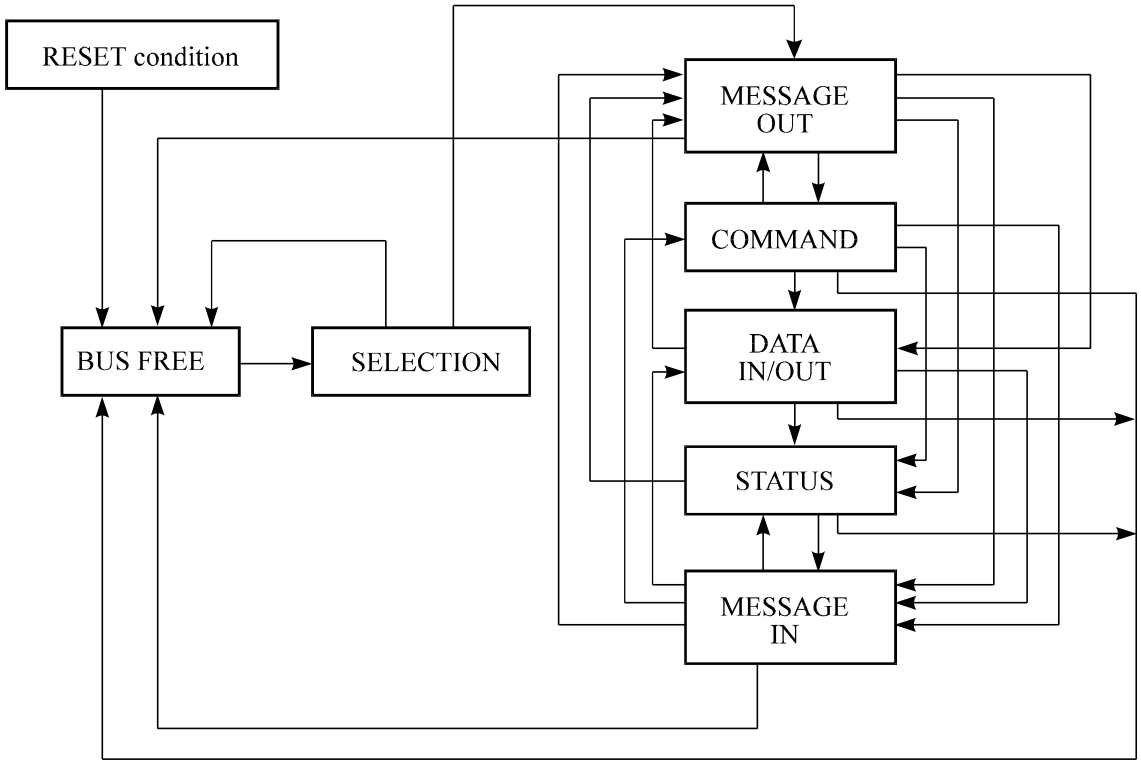


Figure 1.43 Bus phase sequence (1 of 2)

[When ARBITRATION is not used with MESSAGE OUT]



[When ARBITRATION is not used without MESSAGE OUT]

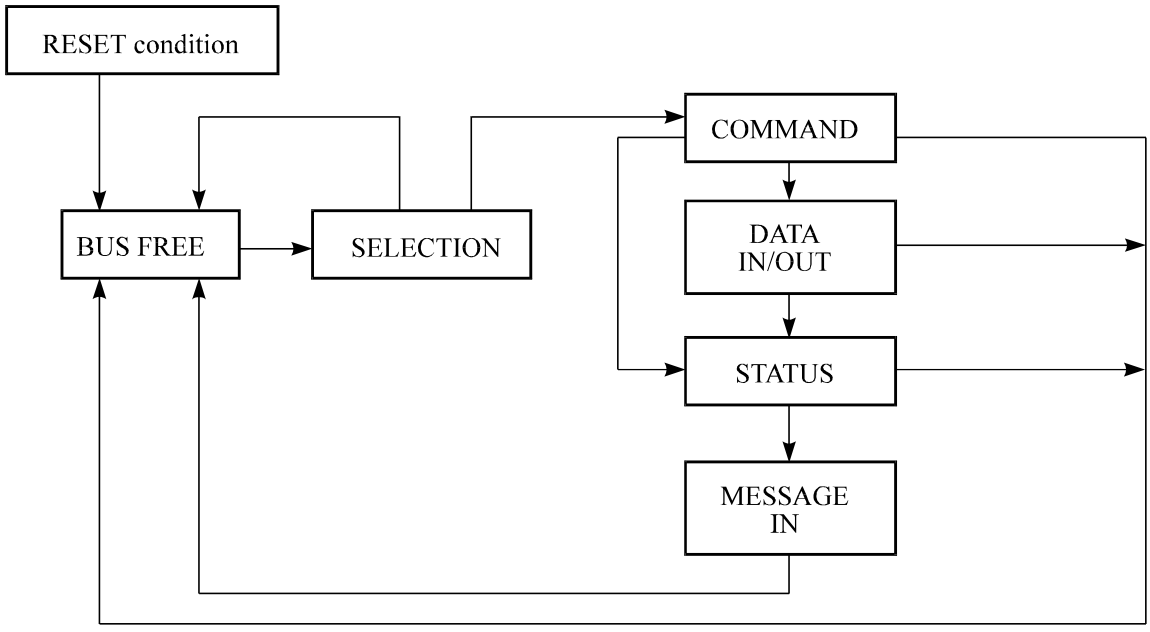


Figure 1.43 Bus phase sequence (2 of 2)

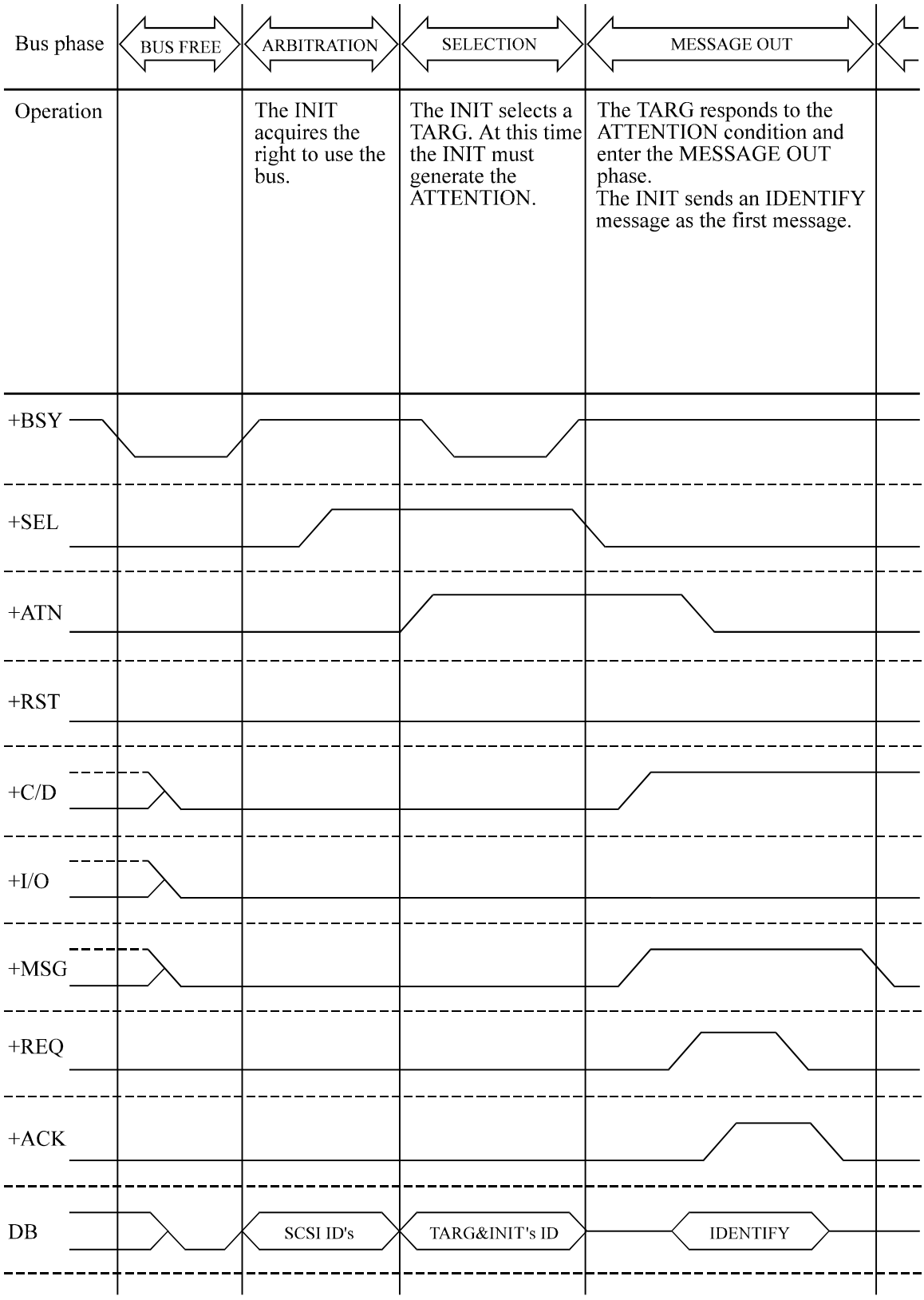


Figure 1.44 Example of bus phase transition at execution of a single command (1 of 5)

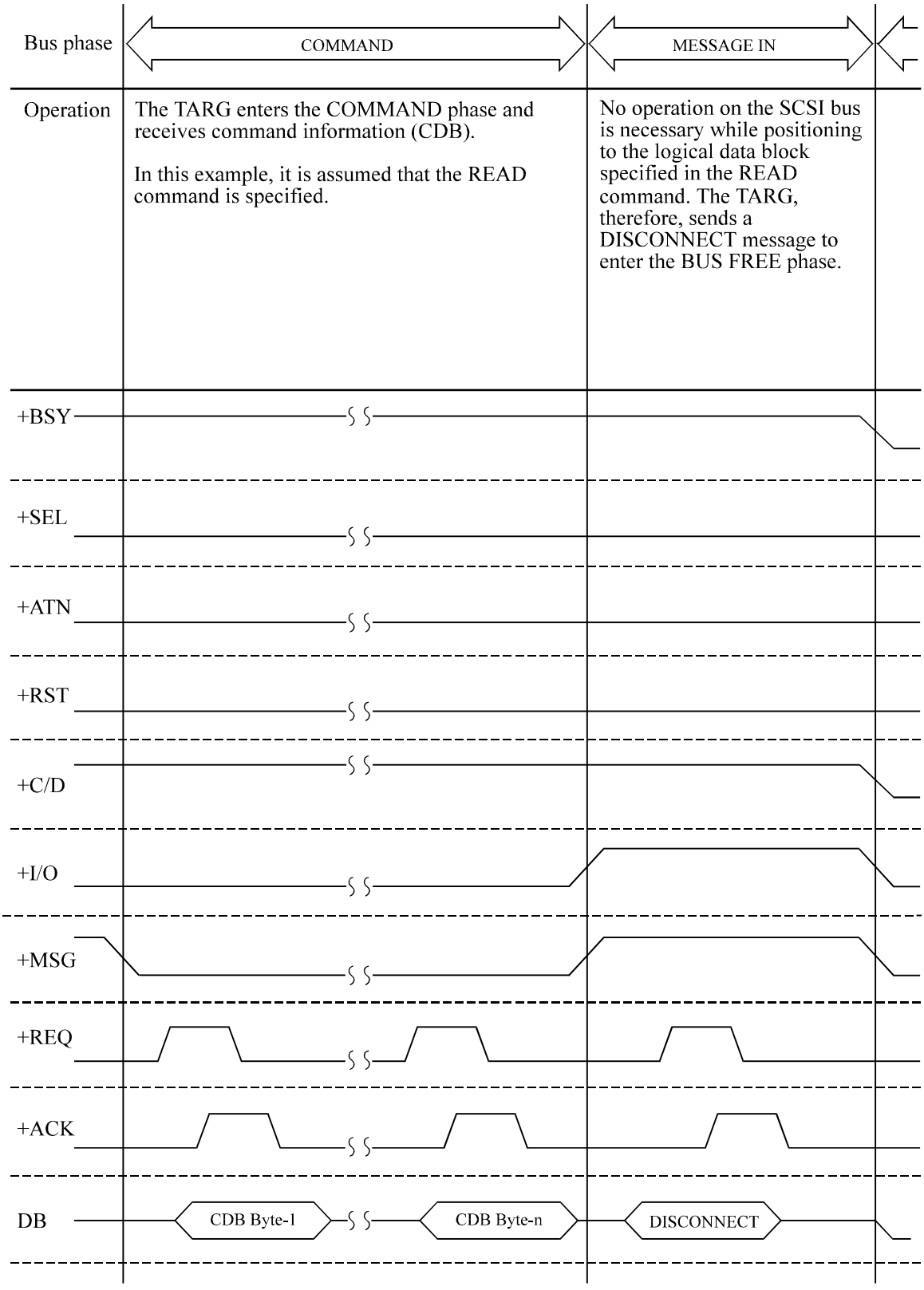


Figure 1.44 Example of bus phase transition at execution of a single command (2 of 5)

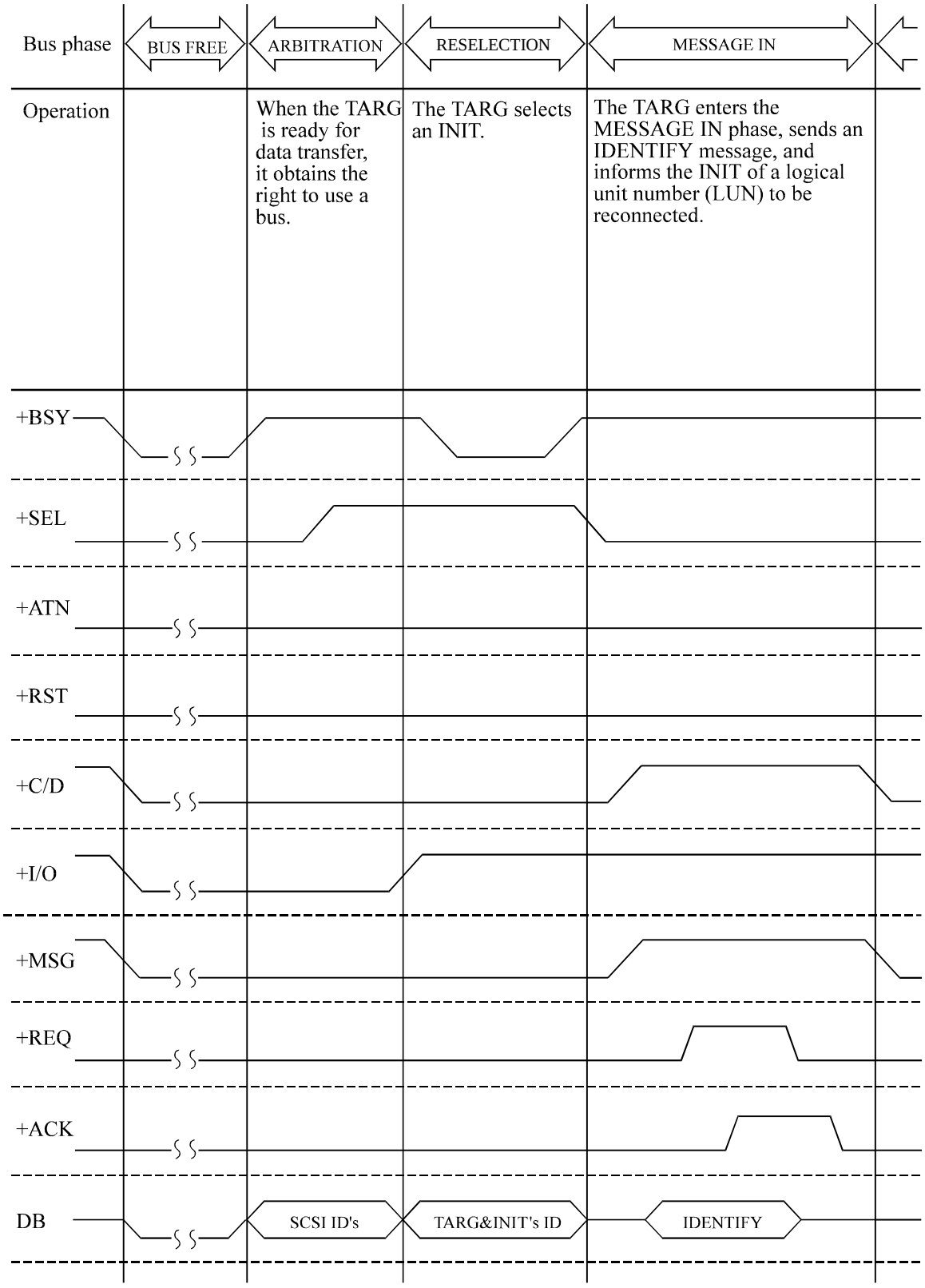


Figure 1.44 Example of bus phase transition at execution of a single command (3 of 5)

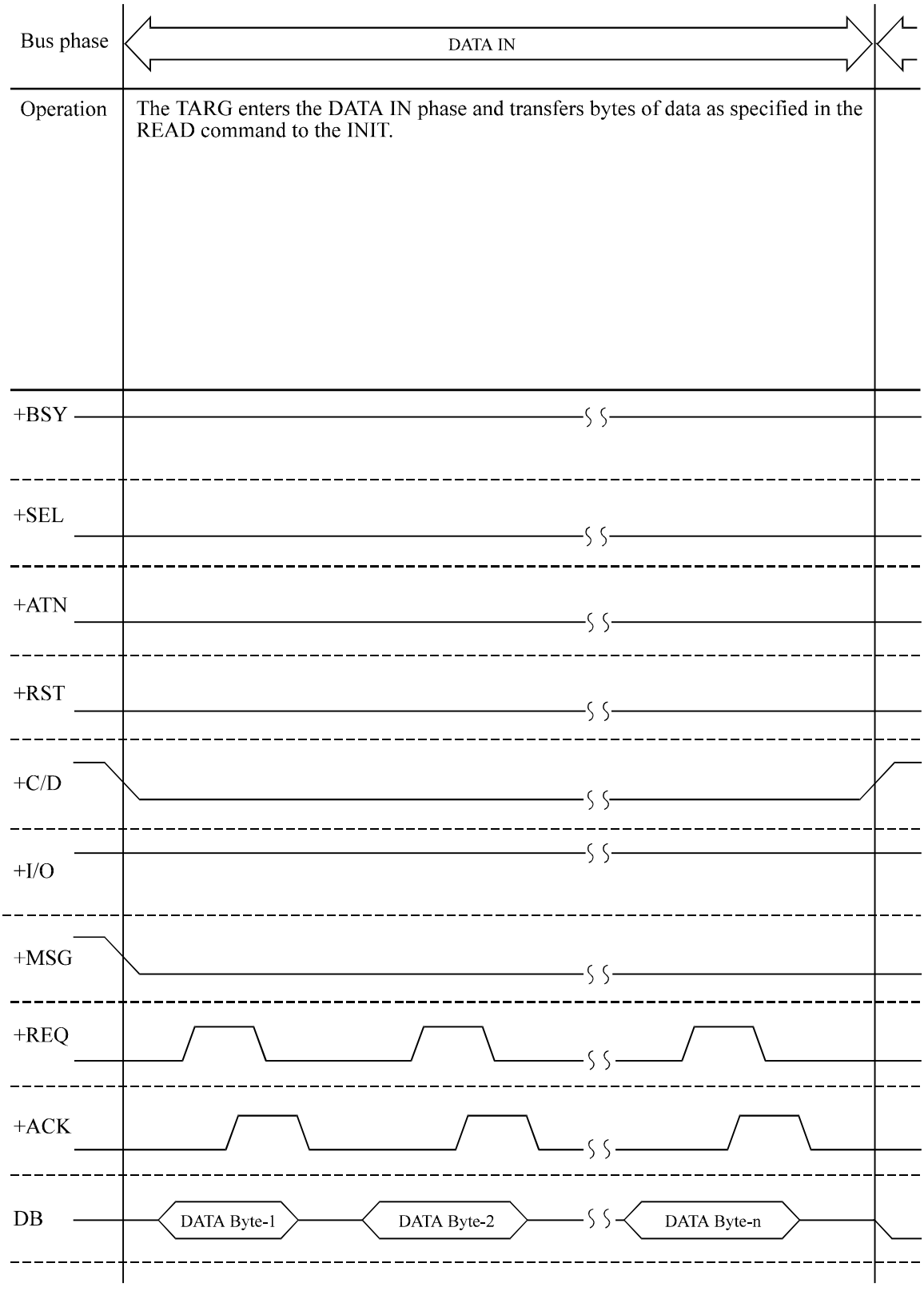


Figure 1.44 Example of bus phase transition at execution of a single command (4 of 5)

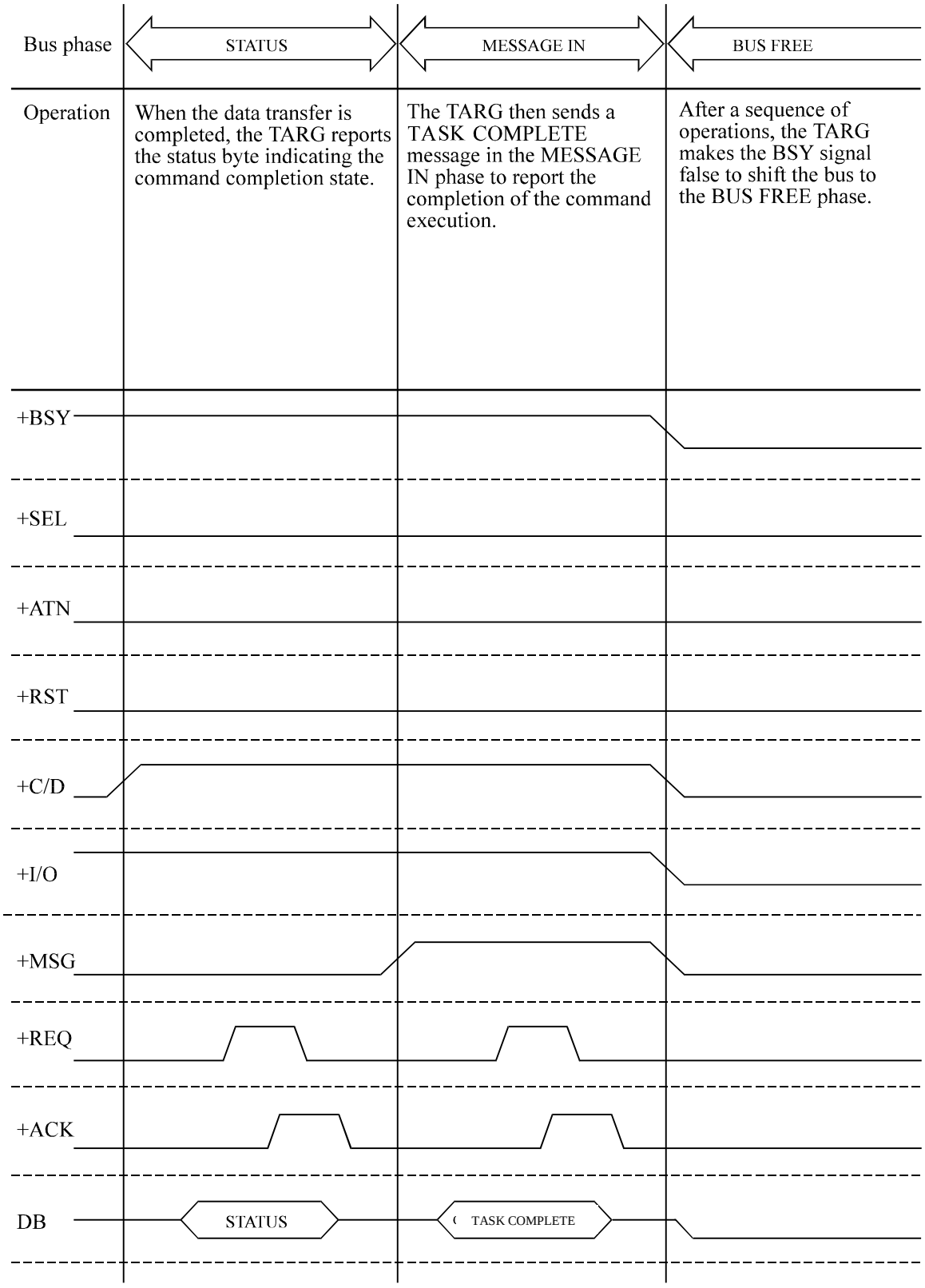


Figure 1.44 Example of bus phase transition at execution of a single command (5 of 5)

1.8.2 Phase sequences with information unit enabled

1.8.2.1 Phase sequences for physical reconnection or selection without using attention condition

The sequences for physical reconnection or selection without using attention condition while an information unit transfer agreement is in effect shall be as shown in Figure 1.45.

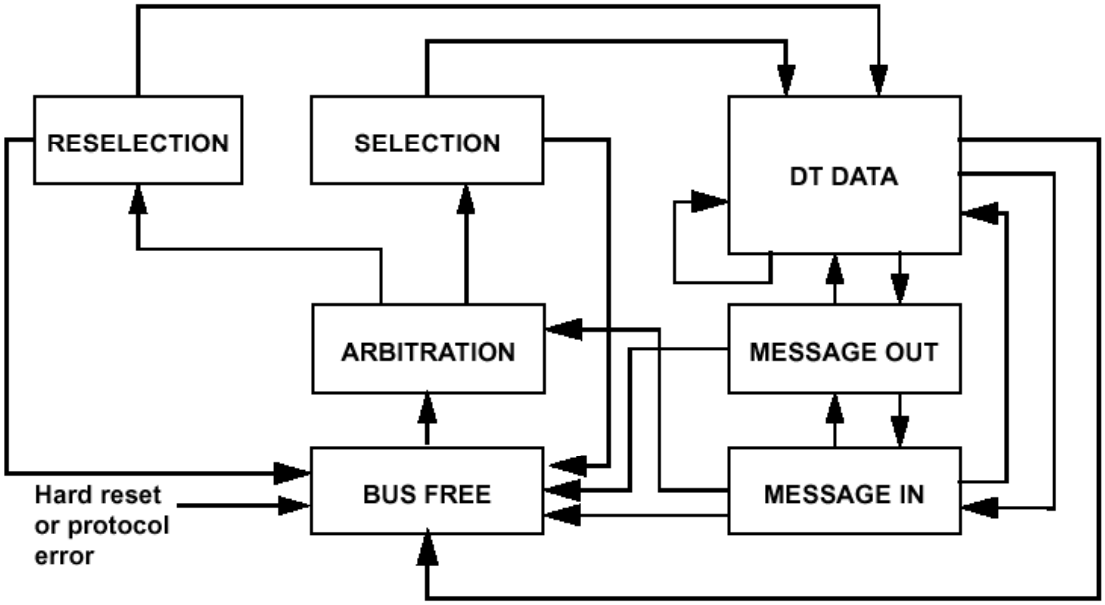
The normal progression for selection without using attention condition (see 10.5.3) if QAS is disabled is:

1) from BUS FREE to ARBITRATION:

2) from ARBITRATION to SELECTION or RESELECTION; and

3) from SELECTION or RESELECTION to one or more DT DATA phases; and

4) from the final DT DATA phase to BUS FREE.



Note: See Figure 1.47, 48, 49, 50 for the sequencing of SPI information units within the DT DATA phases.

Figure 1.45 Phase sequences for physical reconnection or selection without using attentioncondition with information unit transfers enabled

1.8.2.2 Phase sequences for selection using attention condition

The sequences for a selection with attention condition while an information unit transfer agreement is in effect shall be as shown in Figure 1.46.

The normal progression for selection using attention condition (see 10.5.2.3) if QAS is disabled is:

1) from BUS FREE to ARBITRATION;

2) from ARBITRATION to SELECTION;

3) from SELECTION to MESSAGE OUT;

4) from MESSAGE OUT to MESSAGE IN; and

5) from MESSAGE IN to BUS FREE.

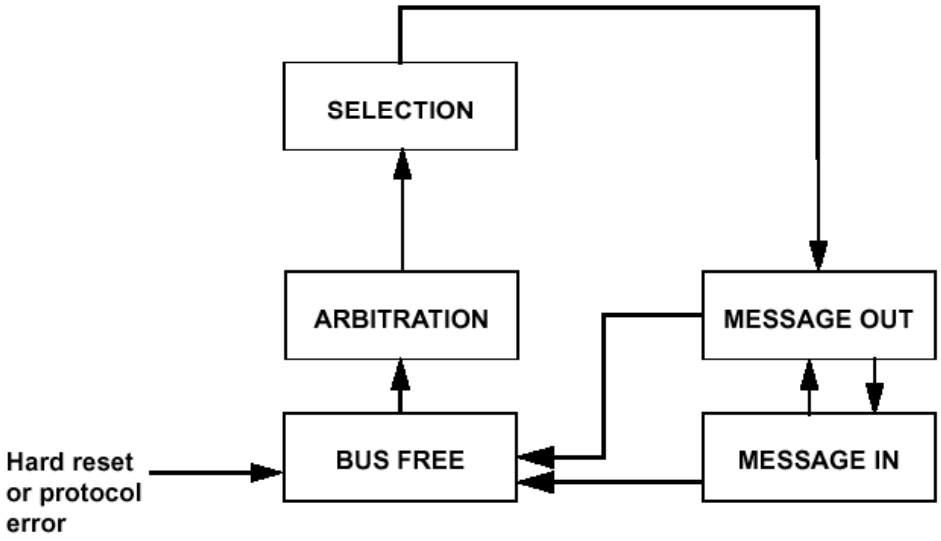


Figure 1.46 Phase sequences for selection with attention condition with information unit transfers enabled

1.9 SPI information units

1.9.1 SPI information unit overview

An information unit transfer transfers data in SPI information units. The order in which SPI information units are transferred within an information unit transfer follows a prescribed sequence. When information unit transfers are enabled only SPI information units shall be transferred within the DT DATA OUT phase and DT DATA IN phase.

The SPI information unit sequences shall be as shown in Figure 1.47, 48, 49, 50. See Figure 1.45 and 1-46 for the sequencing rules between the DT DATA IN or DT DATA OUT phases and the other phases.

The normal progression is from SPI L_Q information unit/SPI command information unit pairs, to SPI L_Q information unit/SPI data information unit pairs, to SPI L_Q information unit/SPI status information unit pairs.

Note :

An INIT may request a BUS FREE phase by creating an attention condition and ending a DISCONNECT message on the corresponding MESSAGE OUT phase. This allows an INIT to request the TARG break up a long sequence of SPI L_Q information unit/SPI ata information unit pairs into smaller sequences.

After message phases complete that contain any negotiation (i.e., PPR or WDTR or SDTR) that results in IU_REQ being changed, the TARG will abort all tasks, except the current task, for the INIT participating in the negotiation and the INIT shall abort all tasks, except the current task, for the TARG.

When an information unit transfer agreement is in effect there is no option equivalent to the "physical disconnect without sending a SAVE DATA POINTERS message." The INIT shall save the data pointers as soon as the last byte of the last iuCRC for a SPI information unit is transferred. The save shall occur even if the INIT detects an error in the SPI data information unit.

The TARG will not start a new information unit transfer until all previous REQ(s) have been responded to by an equal number of ACK(s) except during a sequence of SPI data stream information units.

1.9.2 Information unit transfer logical operations

SCSI devices using information unit transfers may transfer SPI information units for any number of I/O processes by using logical connects, logical disconnects, and logical reconnects.

If there are no phase changes to a MESSAGE OUT phase or a MESSAGE IN phase then logical disconnects shall only occur at the completion of:

a) each SPI command information unit;

b) each SPI status information unit;

c) each SPI data information unit;

d) any SPI L_Q information unit if the SPI L_Q information unit DATA LENGTH field is zero; and

e) the last SPI data stream information unit.

At completion of those SPI information units the I_T_L_Q nexus becomes an I_T nexus. The I_T nexus remains in place until the TARG does a physical disconnect or an I_T_L_Q nexus is reestablished by the TARG transmitting a SPI L_Q information unit.

Logical reconnections occur on the successful TARG transmission and INIT receipt of a SPI L_Q information unit for an existing I/O process. The logical reconnection reestablishes the I_T_L_Q nexus for that I/O process.

SCSI devices using information unit transfers may receive several commands during an initial connection. This occurs when an INIT uses the multiple command option in the SPI L_Q information unit.

For each SPI L_Q received with a multiple command type or a last command type a logical connection occurs and an I_T_L_Q nexus is formed.

If there is a phase change to a MESSAGE OUT phase or a MESSAGE IN phase then there is no logical disconnect and the I_T_L_Q nexus remains in place. If a DT DATA phase follows the message phase then the L_Q portion of the current I_T_L_Q nexus shall be replaced with the L_Q in the next SPI L_Q information unit.

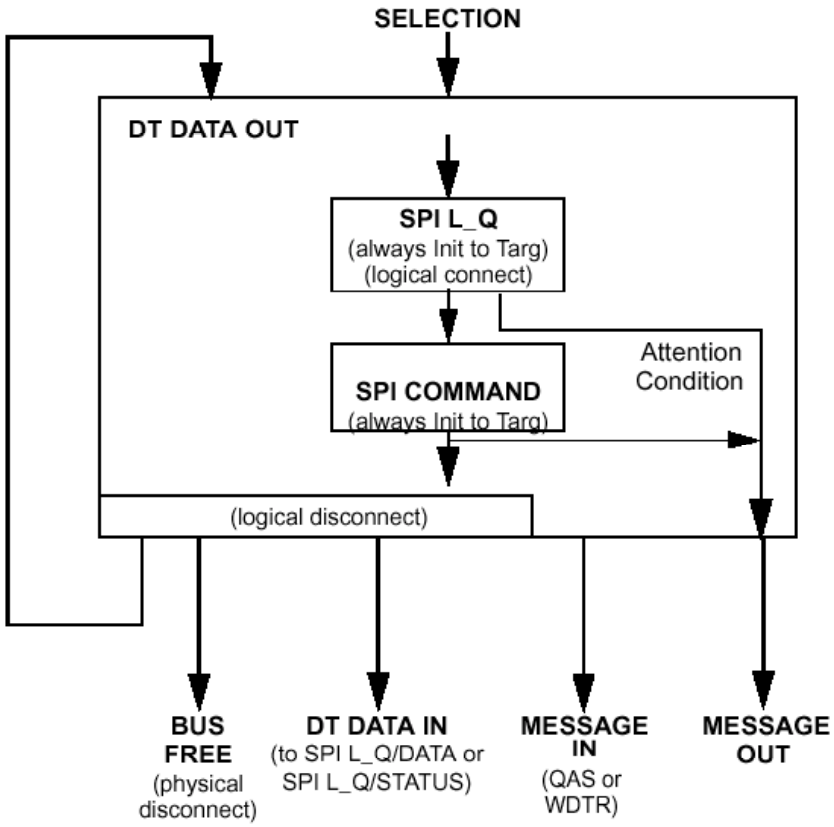


Figure 1.47 SPI information unit sequence during initial connection

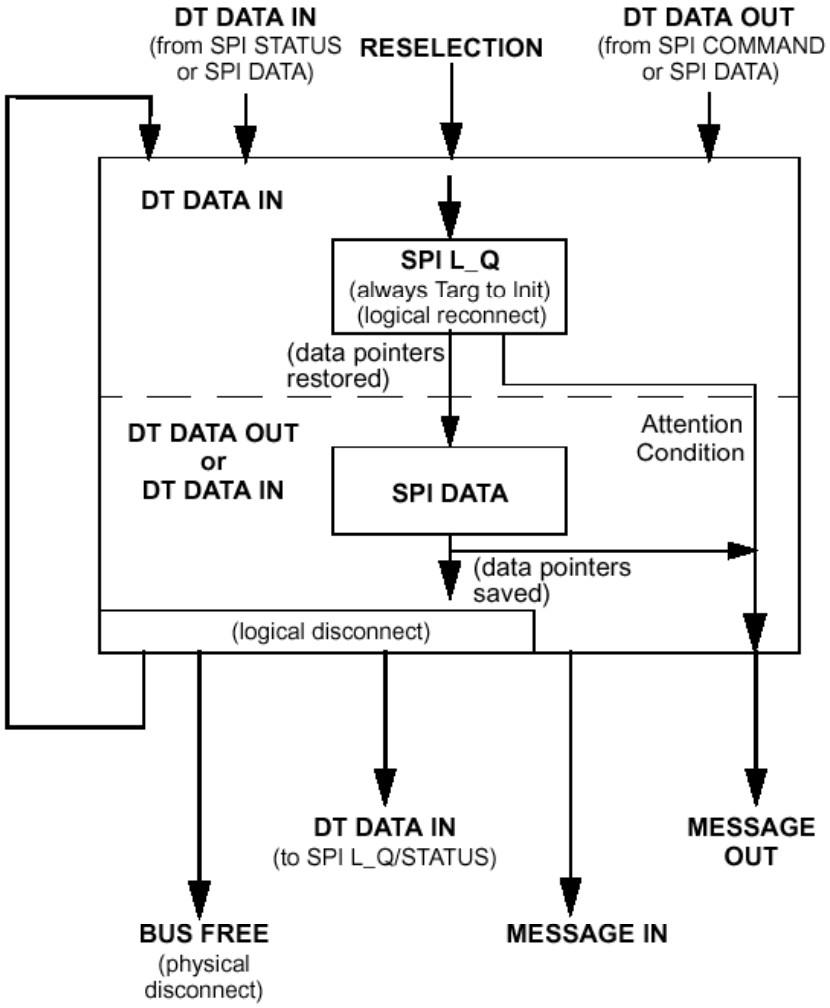


Figure 1.48 SPI information unit sequence during data type transfers

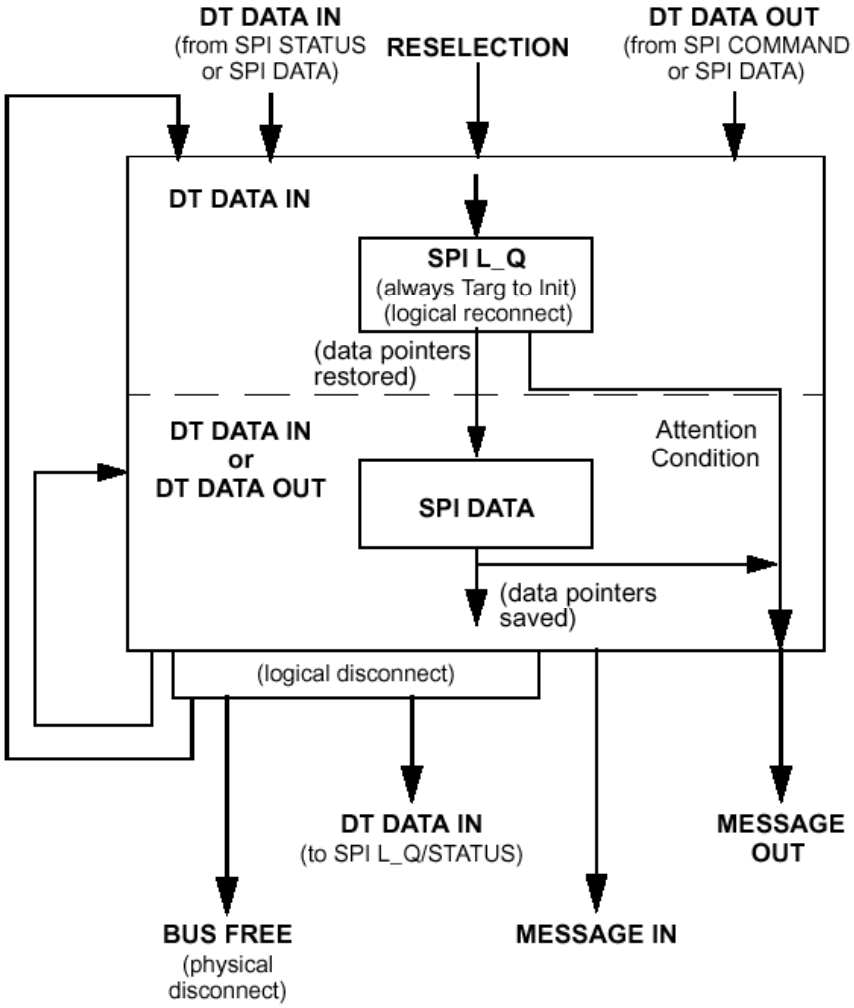


Figure 1.49 SPI information unit sequence during data stream type transfers

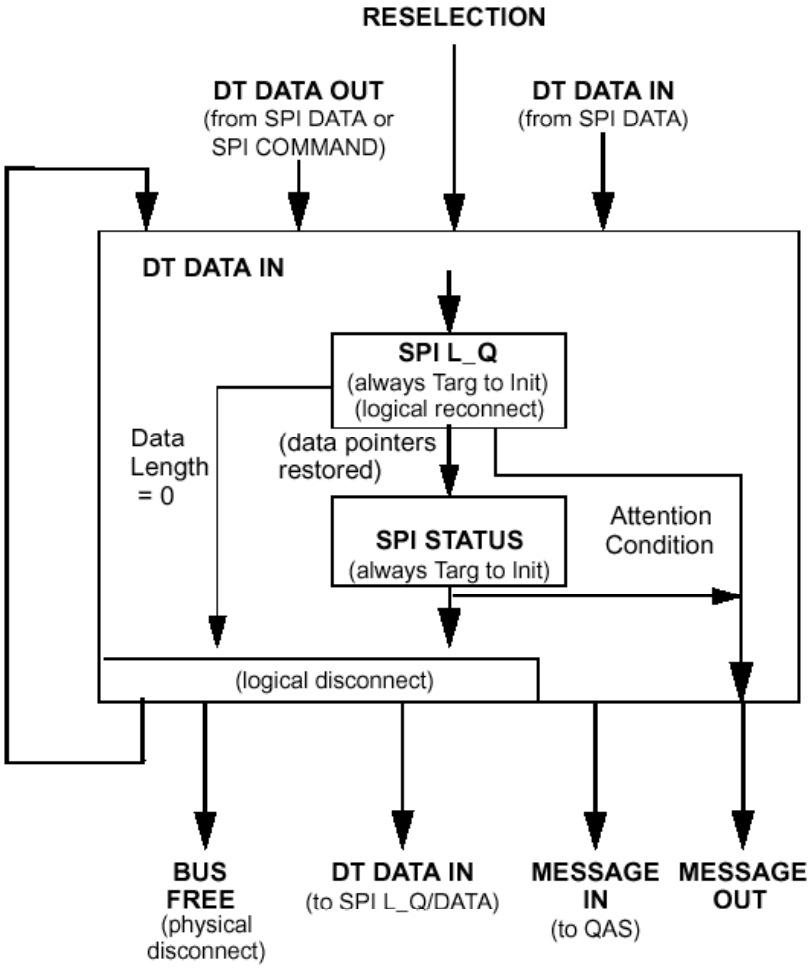


Figure 1.50 SPI information unit sequence during status transfers

1.9.3 SPI information units

1.9.3.1 SPI command information unit

The SPI command information unit (see table 1.22) transfers CDBs, task attributes, and task management requests to be performed by a device server.

An INIT shall consider a BUS FREE phase after the transfer of a SPI command information unit to be equivalent to receiving a DISCONNECT message.

If a TARG does not have the resources to accept a SPI command information unit and the TASK MANAGEMENT FUNCTIONS field equals 00h the TARG transfers all the bytes of the current SPI command information unit and discards the transmitted information. After transferring all the SPI command information unit bytes the TARG will transmit a SPI L_Q/SPI status information unit pair with the status defined in the ***SCSI Architecture Model-2*** standard for this condition. This SPI status information unit may be transferred in the same or a subsequent connection. If the INIT has more commands to send to the TARG, the INIT shall wait at least until the next selection before those remaining commands may be sent.

If the TASK MANAGEMENT FUNCTIONS field is a supported value not equal to 00h the TARG performs the selected task management function before processing any further SPI information units regardless of the command type. On completion of a supported task management function the TARG goes to a BUS FREE phase. No SPI status information unit shall be reported for the task management function. If the TASK MANAGEMENT FUNCTIONS field is not a supported value then the task manager shall terminate the task with a GOOD status and the packetized failure code shall be set to TASK MANAGEMENT FUNCTION NOT SUPPORTED. If a task management function fails the task manager shall terminate the task with a GOOD status. The packetized failure code shall be set to TASK MANAGEMENT FUNCTION FAILED.

If the TARG terminates a SPI L_Q/SPI command information unit pair for one of the following reasons:

a) TASK SET FULL status,

b) BUSY status,

c) CHECK CONDITION due to a SPI command information unit iuCRC error, or

d) a bus free due to a SPI L_Q information unit iuCRC error it shall have no effect on any other SPI L_Q/SPI command information unit pair beyond those caused by any task management functions contained within the last SPI L_Q/SPI command information unit pair.

Table 1.22 SPI command information unit

Bit Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved					TASK ATTRIBUTE		
2	TASK MANAGEMENT FUNCTIONS							
3	ADDITIONAL CDB LENGTH = (number of additional CDB bytes)/4						***RDDATA***	***WRDATA***
4	CDB							
19								
20	ADDITIONAL CDB							
N								
n+1	(MSB)	IUCRC						
n+2								
n+3								
n+4								(LSB)

The TASK ATTRIBUTE field is defined in table 1.23.

Table 1.23 TASK ATTRIBUTE

Codes	Description
000b	Requests that the task be managed according to the rules for a simple task attribute. (See the SCSI Architecture Model-2 standard)
001b	Requests that the task be managed according to the rules for a head of queue task attribute. (See the SCSI Architecture Model-2 standard)
010b	Requests that the task be managed according to the rules for an ordered attribute. (See the SCSI Architecture Model-2 standard)
011b	Reserved
100b	Requests that the task be managed according to the rules for an automatic contingent allegiance task attribute. (See the SCSI Architecture Model-2 standard)
101b-111b	Reserved

The TASK MANAGEMENT FUNCTIONS field is defined in table 1.24. If a task management function fails the task manager shall terminate the task with a GOOD status. The packetized failure code shall be set to TASK MANAGEMENT FUNCTION FAILED.

Table 1.24 TASK MANAGEMENT FUNCTIONS

Codes	Description
00h	Indicates no task management requests for the current task.
01h	The task manager shall abort the task as defined in the ABORT TASK Message.
02h	The task manager shall abort the task set as defined in the ABORT TASK SET message.
04h	The task manager shall clear the task set as defined in the CLEAR TASK SET message.
08h	The task manager shall perform a logical unit reset of the selected logical unit as defined in the LOGICAL UNIT RESET message.
20h	The task manager shall perform a target reset as defined in the TARGET RESET message.
40h	The task manager shall perform a clear ACA as defined in the CLEAR ACA message.
All other values reserves	The task manager shall terminate the task with a GOOD status. The packetized failure code shall be set to TASK MANAGEMENT FUNCTION NOT SUPPORTED.

The ADDITIONAL CDB LENGTH field contains the length in 4-byte words of the ADDITIONAL CDB field.

The write data (WRDATA) bit and read data (RDDATA) bit are not supported.

The CDB field contains the actual CDB to be interpreted by the addressed logical unit. The CDB field and the task attribute field is not valid and is ignored if the TASK MANAGEMENT FUNCTIONS field is not zero. Any bytes between the end of a 6 byte CDB, 10 byte CDB, or 12 byte CDB and the end of the CDB field shall be reserved.

The ADDITIONAL CDB field contains any CDB bytes beyond those contained within the standard 16 byte CDB field.

The CDB field, ADDITIONAL CDB field, and TASK ATTRIBUTE field are not valid and are ignored if the TASK MANAGEMENT FUNCTIONS field is not zero.

The contents of the CDB and ADDITIONAL CDB fields shall be as defined in the ***SCSI command standards***.

1.9.3.2 SPI L_Q information unit

The SPI L_Q information unit (see table 1.25) contains L_Q nexus information for the information unit that follows, the type of information unit that follows, and the length of information unit that follows. A SPI L_Q information unit shall precede all SPI command information units, SPI multiple command information units, SPI data information units, SPI status information units, and the first of an uninterrupted sequence of SPI data stream information units.

The receipt of an error free (i.e., no iuCRC error) SPI L_Q information unit by an INIT shall cause the INIT to restore the data pointers.

Table 1.25 SPI L_Q information unit

Bit Byte	7	6	5	4	3	2	1	0
0	TYPE							
1	Reserved							
2	(MSB)			TAG				
3								(LSB)
4	(MSB)			LOGICAL UNIT NUMBER				
11								(LSB)
12	Reserved							
13	(MSB)			DATA LENGTH				
14								
15								(LSB)
16	DIDI DIRECTION		Reserved					
17	Reserved							
18	(MSB)			IUCRC INTERVAL				
19								(LSB)
20	(MSB)			IUCRC				
21								
22								
23								(LSB)

The TYPE field is defined in table 1.26. If a INIT receives a type code that is not defined in table 1.26 that INIT shall follow the procedures defined in ***1.6.5.3 (6) (a)***. If a TARG receives a type code that is not defined in table1.26 that TARG follows the procedures defined in ***1.6.5.3 (6) (b)***.

Table 1.26 TYPE

Codes	Type	Description
01h	**Last Command**	Sent by a SCSI initiator device to indicate a SPI command information unit shall follow this SPI L_Q information unit. Indicates the SCSI initiator device shall not send any more SPI command information units during the current connection. The value of the DATA LENGTH field shall be greater than or equal to 14h and less than or equal to 90h. The IUCRC INTERVAL field shall be set to zero and ignored by the SCSI target device. The BIDI DIRECTION field shall be set to zero and ignored by the receiving SCSI target device.
02h	**Multiple Command**	Sent by a SCSI initiator device to indicate a SPI command information unit shall follow this SPI L_Q information unit. Indicates the SCSI initiator device has another SPI L_Q information unit and SPI command information unit during the current connection. The value of the DATA LENGTH field shall be greater than or equal to 14h and less than or equal to 90h. The IUCRC INTERVAL field shall be set to zero and ignored by the SCSI target device. The IUCRC INTERVAL field shall be set to zero and ignored by the SCSI target device. The BIDI DIRECTION field shall be set to zero and ignored by the receiving SCSI target device.
04h	**Data**	Sent by a SCSI target device to indicate a SPI data information unit shall follow this SPI L_Q information unit. The DATA LENGTH field shall not be set to zero. For a bidirectional command, the direction of the SPI data information unit shall be indicated in the BIDI DIRECTION field of the SPI L_Q in-formation unit as defined in table 1.27.
05h	**Data Stream**	Sent by a SCSI target device to indicate an unspecified number of SPI data stream information unit shall follow this SPI L_Q information unit. The DATA LENGTH field shall not be set to zero. For a bidirectional command, the direction of the SPI data stream information units shall be indicated in the BIDI DIRECTION field of the SPI L_Q information unit as defined in table 1.27.
08h	**Status**	Sent by a SCSI target device to indicate a SPI status information unit may follow this SPI L_Q information unit. A length of zero in the DATA LENGTH field shall indicate no SPI status information unit shall follow the SPI L_Q information unit (see 1.9.3.5). The IUCRC INTERVAL field shall be set to zero and ignored by the SCSI initiator device. The IUCRC INTERVAL field shall be set to zero and ignored by the SCSI target device. The BIDI DIRECTION field shall be set to zero and ignored by the receiving SCSI initiator device.
F0h - FFh		Vendor specific
All others		Reserved

The TAG field is a 16-bit integer assigned by the application client and sent to the INIT in the send SCSI command request.

The LOGICAL UNIT NUMBER field specifies the address of the logical unit of the I_T_L_Q nexus for the current task. The structure of the logical unit number field shall be as defined in the ***SCSI Architecture Model-2*** standard. If the addressed logical unit does not exist, the task manager shall follow the SCSI rules for selection of invalid logical units as defined in the ***SCSI Primary Commands-3*** standard.

The DATA LENGTH field contains the length in bytes of the following information units. For SPI data stream information units the data length field contains the length in bytes of each SPI data stream information unit that follows (i.e., the total number of bytes transferred would equal the data length times the number of SPI data stream information units transferred). The data length shall not include any of the 4 byte iuCRC nor any transmitted pad bytes (e.g., a data length of 509 with a iuCRC interval of zero or greater than 509 would transfer 509 bytes of data plus 3 bytes of pad plus 4 bytes of iuCRC for a total transfer of 516 bytes). The TARG will not set the data length to a value that exceeds the maximum burst size as defined in the disconnect-reconnect page.

The BIDI DIRECTION field determines the data direction if the command is a bidirectional command and the type code is data or data stream. The code values for the BIDI DIRECTION field are defined in table 1.27.

Table 1.27 BIDI DIRECTION

Codes	Description
00b	A unidirectional command or a type code other than data or data stream. (see table 1.26)
01b	A bidirectional command transferring data from the SCSI initiator device to the SCSI target device.
10b	A bidirectional command transferring data from the SCSI target device to the SCSI initiator device.
11b	Reserved.

The IUCRC INTERVAL field contains the length in bytes of the data to be sent before a iuCRC is transferred. The iuCRC interval length shall not include the 4 byte iuCRC nor any transmitted pad bytes (e.g., an iuCRC interval length of 510 transfer 510 bytes of data plus 2 bytes of pad plus 4 bytes of iuCRC for a total transfer of 516 bytes). The iuCRC interval shall be a multiple of two (i.e., odd numbers are not allowed). If the iuCRC interval is equal to zero or is greater than or equal to the data length only one iuCRC shall occur at the end of the SPI information unit.

1.9.3.3 SPI data information unit

The SPI data information unit (see table 1.28) contains data.

The detection of a BUS FREE phase following a SPI data information unit by an INIT shall be equivalent to the INIT receiving a DISCONNECT message.

The detection of a QAS REQUEST message following a SPI data information unit by a INIT shall be equivalent to the INIT receiving a DISCONNECT message.

Table 1.28 SPI data information unit

Bit Byte	7	6	5	4	3	2	1	0
0	DATA							
N								
N+1	(MSB)							
N+2	IUCRC							
N+3								
N+4								(LSB)

The DATA field may contain any type of information (e.g., parameter lists, mode pages, user data).

If the IUCRC INTERVAL field of the SPI L_Q information unit contains a value greater than zero and less than the data length then there is an IUCRC field at each iuCRC interval in addition to the iuCRC shown in table 1.28. These additional IUCRC fields are not shown in table 1.28.

1.9.3.4 SPI data stream information unit

The SPI data stream information unit (see table 1.29) contains data.

All the SPI data stream information units transferred after a SPI L_Q information unit with a type of data stream shall be the size indicated in the DATA LENGTH field of the SPI L_Q information unit.

If the data transfer size is not a multiple of the data length, the TARG ends the stream at a data length boundary and sends a new SPI L_Q with a smaller data length to finish the data transfer.

The new SPI L_Q may or may not be sent during the current physical connection.

During write streaming the sequence of SPI data stream information units shall end with any change to the C/D, I/O, or MSG signals on a SPI data stream information unit boundary. If during write streaming SPI data stream information units an INIT detects a REQ transition after transmitting the last iuCRC for a SPI data stream information unit that INIT shall transmit the next SPI data stream information unit.

During read streaming the TARG ends a sequence of SPI data stream information units by performing one of the following:

a) should assert the P_CRCA signal before the end of the current SPI data stream information unit boundary; or

b) may change the C/D, I/O, or MSG signals on a SPI data stream information unit boundary.

If during the last SPI data stream information unit, of a read stream, the P_CRCA signal was not asserted and an INIT detects a REQ transition after receiving the last iuCRC for a SPI data stream information unit that INIT shall receive the next SPI data stream information unit. If during the last SPI data stream information unit the P_CRCA signal was asserted and an INIT detects a REQ transition after receiving the last iuCRC for a SPI data stream information unit that INIT shall logically disconnect from the current I_T_L_Q nexus.

If during a sequence of SPI data stream information units an INIT detects any change to the C/D, I/O, or MSG signals after transmitting or receiving the last iuCRC for a SPI data stream information unit that INIT shall consider the current I/O process to be logically disconnected or in the case of detecting a BUS FREE phase or a MESSAGE IN phase to be physically disconnected.

The detection of a BUS FREE phase following a SPI data stream information unit by an INIT shall be equivalent to the INIT receiving a DISCONNECT message.

The detection of a QAS REQUEST message following a SPI data stream information unit by an INIT shall be equivalent to the INIT receiving a DISCONNECT message.

To end a sequence of SPI data stream information units an INIT may request a disconnect by establishing an attention condition. The INIT shall continue to transfer or receive data, pad bytes (if any), and iuCRC(s) until the TARG changes to the MESSAGE OUT phase.

During a sequence of SPI data stream information units the offset count is not required to go to zero at the boundary of any SPI data stream information unit if the next SPI information unit is a SPI data stream information unit.

Table 1.29 SPI data stream information unit

Bit Byte	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	DATA							
n								
2	(MSB)							
3				IUCRC				
4								
11								(LSB)

The DATA field may contain any type of information (e.g., parameter lists, mode pages, user data).

If the IUCRC INTERVAL field of the SPI L_Q information unit contains a value greater than zero and less than the data length then there is an IUCRC field at each iuCRC interval in addition to the iuCRC shown in table 1.29. These additional IUCRC fields are not shown in table 1.29.

1.9.3.5 SPI status information unit

The SPI status information unit (see table 1.30) contains the completion status of the task indicated by the preceding SPI L_Q information unit. The TARG considers the SPI status information unit transmission to be successful when there is no attention condition on the transfer of the information unit.

If a task completes with a GOOD status, a SNSVALID bit of zero, and a RSPVALID bit of zero then the TARG shall set the DATA LENGTH field in the SPI L_Q information unit to zero.

Table 1.30 SPI status information unit

Bit Byte	7	6	5	4	3	2	1	0
0	DATA							
1	RESERVED							
2	RESERVED FOR FCP						SNSVALID	RSPVALID
3	STATUS							
4	(MSB)	SENSE DATA LIST LENGTH(n-m)						
7								(LSB)
8		PACKETIZED FAILURES LIST LENGTH(m-11)						
11								
12		PACKETIZED FAILURES						
M								
M+1	SENSE DATA							
N								
N+1	(MSB)	IUCRC						
N+2								
N+3								
N+4								(LSB)

A sense data valid bit (SNSVALID) of zero indicates the sense data list length shall be ignored and no sense data is provided. A SNSVALID bit of one indicates the SENSE DATA LIST LENGTH field specifies the number of bytes in the SENSE DATA field. If the STATUS field contains a CHECK CONDITION status the SNSVALID bit will be set to one.

If sense data is provided, SNSVALID will be set to one and the SENSE DATA LIST LENGTH field will specify the number of bytes in the SENSE DATA field. The SENSE DATA LIST LENGTH field only contains even lengths greater than zero and not be set to a value greater than 252.

If no sense data is provided, SNSVALID shall be set to zero. The INIT shall ignore the SENSE DATA LIST LENGTH field and shall assume a length of zero.

If packetized failure data is provided, the packetized failures valid bit (RSPVALID) will be set to one and the PACKETIZED FAILURES LIST LENGTH field will specify the number of bytes in the PACKETIZED FAILURES field.

The PACKETIZED FAILURES LIST LENGTH field contains a length of 4. Other lengths are reserved for future standardization.

If no packetized failure data is provided, RSPVALID will be set to zero. The INIT shall ignore the PACKETIZED FAILURES LIST LENGTH field and shall assume a length of zero.

The STATUS field contains the status of a task that completes. See the ***SCSI Architecture Model-2*** standard for a list of status codes.

The PACKETIZED FAILURES field (see table 1.31) contains information describing the packetized failures detected during the execution of a task. The PACKETIZED FAILURES field shall contain valid information if the TARG detects any of the conditions described by the packetized failure code (see table 1.32).

Table 1.31 PACKETIZED FAILURES field

Bit Byte	7	6	5	4	3	2	1	0
0	RESERVED							
1	RESERVED							
2	RESERVED							
3	PACKETIZED FAILURE CODE							

The PACKETIZED FAILURE CODE field is defined in table 1.31.

Table 1.32 PACKETIZED FAILURE CODE

Codes	Description
00h	NO FAILURE
01h	Reserved
02h	SPI COMMAND INFORMATION UNIT FIELDS INVALID
03h	Reserved
04h	TASK MANAGEMENT FUNCTION NOT SUPPORTED
05h	TASK MANAGEMENT FUNCTION FAILED
06h	INVALID TYPE CODE RECEIVED IN SPI L_Q INFORMATION UNIT
07h	ILLEGAL REQUEST RECEIVED IN SPI L_Q INFORMATION UNIT
11h	Reserved.

The SENSE DATA field contains the information specified by the ***SCSI Primary Commands-3*** standard for presentation by the REQUEST SENSE command. The proper sense data shall be presented when a SCSI status byte of CHECK CONDITION is presented as specified by the ***SCSI Primary Commands-3*** standard.

1.10 SCAM

The IDD does not support the SCAM functions.

1.10.1 SCAM operations

The SCAM operation functions include all functions required for ID assignment of each SCAM device so that the SCAM tolerant and SCAM devices are identified by the SCAM initiator and target. The user shall understand the SCAM operations clearly by knowing the operations between the SCAM initiator and target.

(1) SCAM initiator

The SCAM initiator shall complete its local initialization immediately after the power-on. It shall wait at least a SCAM power-on to the SCAM selection delay before initiating any SCSI bus activity. The SCAM initiator, which can be a level-1 SCAM device or can be determined to be the dominant SCAM initiator, shall generate a RESET condition immediately after power-on. The level-2 SCAM initiator, which cannot be determined to be the dominant SCAM initiator by the deductive method, shall not generate a RESET condition. However, it shall start the SCAM protocol as if it has detected the RESET condition as described below.

When the SCAM initiator generates or detects a RESET condition, it shall start the SCAM protocol. The first function sequence shall be the Dominant Initiator Contention function. The SCAM initiator becomes the dominant SCAM initiator when it broadcasts the numerically highest ID character string during separation. The SCAM initiator which does not have the highest ID character string is set to a subaudinate SCAM initiator.

Notes:

The level-1 SCAM initiator is not always required for execution of the Dominant Initiator Contention function. It shall be used to detect the Dominant Initiator Contention function which is broadcasted by another SCAM initiator.

The ID character string of the level-1 SCAM initiator has been defined not to be selected through contention by the level-2 SCAM initiator. Therefore, the level-1 SCAM initiator which has failed in contention shall function as the subordinate SCAM initiator.

The level-2 SCAM initiator is always active so that it can detect the SCAM protocol started by another level-2 SCAM unit (the initiator or target).

a. Dominant SCAM initiator

The dominant SCAM initiator shall classify the allowable SCSI IDs into the already assigned group or unassigned group. Also, it shall assign an ID to each SCAM device if necessary. After ID assignment, the dominant SCAM initiator shall broadcast the Configuration Process Complete function. This function sequence is used for two purposes: the report to the subordinate SCAM initiator that it can restart the normal SCSI operations, and the acknowledge to no response to the normal SCSI selection. It indicates that the SCAM target having an unassigned ID keeps its current status.

The dominant SCAM initiator can classify and assign SCSI IDs in various ways as described below.

- SCSI ID classification

  After the reset, the dominant SCAM initiator waits for a certain period to establish a delay time between the reset and selection of SCAM tolerant. The dominant SCAM initiator initializes the SCSI ID internal table and indicates that all SCSI IDs are not classified yet. Also, the SCAM initiator gets the arbitration and selects the unclassified IDs whose selection timeout delay is greater than the response time of SCAM tolerant selection but less than the response delay of SCAM unassigned ID selection. If the dominant SCAM initiator has an already assigned ID, it can start arbitration using this ID. If it does not have the assigned ID, it starts arbitration without IDs.

  When the dominant SCAM initiator detects a selection timeout, it classifies the ID to be unassigned. When the SCSI device responds to the selection by asserting the BSY signal, the dominant SCAM initiator classifies this ID to be already assigned. In this case, the dominant SCAM initiator shall complete the INQUIRY or similar command sequence to normally terminate the SCSI device selection.

  The dominant SCAM initiator shall repeat this process until all SCSI IDs are classified to be assigned or unassigned. Note that the SCSI IDs can be classified even outside of applicable clause of configuration parameters. This can eliminate the requirement of SCSI ID classification.

- SCSI ID assignment

  After all SCSI IDs have been classified, the dominant SCAM initiator shall start the SCAM protocol and repeat ID assignment to all SCSI devices. The dominant SCAM initiator shall execute the Dominant Initiator Contention function sequence to prove that the initiator is still dominant by itself. If the previously dominant SCAM initiator fails in contention with other dominant initiators, it shall continue to control the SCAM protocol but shall function as a slave SCAM initiator.

  After the SCSI ID assignment, the dominant SCAM initiator shall broadcast the Configuration Process Complete function sequence using one or more SCAM protocol instances, and shall terminate the SCAM protocol.

b. Subaudinate SCAM initiator

The subaudinate SCAM initiator shall continue to control the SCAM protocol and shall respond to all of SCAM function sequence. The SCSI ID assignment by the subaudinate SCAM initiator is required for the dominant SCAM initiator to assign its SCSI IDs. Despite of the SCAM target, the subaudinate SCAM initiator needs not stop SCAM protocol control by releasing all signals if it has assigned an SCSI ID. Instead, the subaudinate SCAM initiator shall recognize the sync pattern and the Configuration Process Complete function sequence.

If the subaudinate SCAM initiator has detected the end of SCAM protocol but has failed to recognize the Configuration Process Complete function sequence, it shall not restart the normal SCSI operations. The level-2 SCAM initiator can continue to detect the start of SCAM protocol.

(2) Level-1 SCAM target

Figure 1.51 shows the operations of level-1 SCAM target. Its status names are explained later. The RESET condition can terminate all operations in any status, and it forces the SCAM target to the Reset Delay status.

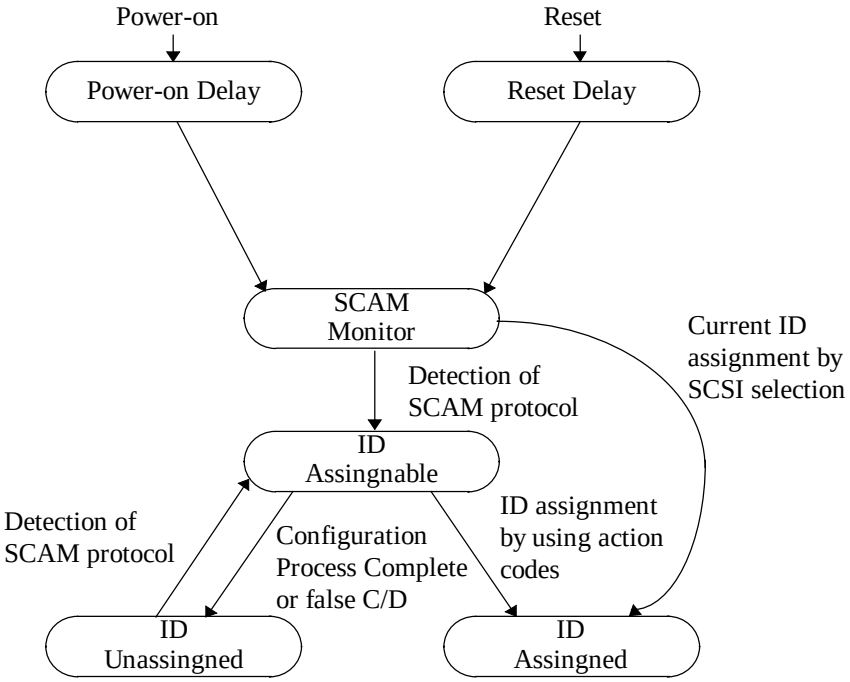


Figure 1.51 State of level-1 SCAM target

The SCAM target enters the Power-On Delay status immediately after the power-on, and allows the local initialization to start. The SCAM target shall exit this status, and enter the SCAM Monitor status within the delay time between SCAM power-on and SCAM selection.

During SCAM Monitor status, the SCAM target shall monitor the SCSI bus for both SCAM selection and normal SCSI selection. When the SCAM target detects the start of SCAM protocol, it shall enter the ID Assignable status. If the SELECTION phase of the current IDs of SCAM target continues to valid during at least the response delay of SCAM unassigned ID selection, this SCAM target shall respond to the selection and assert the BSY signal. The SCAM target shall implicitly enter the ID Assigned status as if its ID assignment was explicitly accepted. The assigned ID is set as the current ID, and the SCAM target functions as the SCAM tolerant device.

The SCAM target continues in the ID Assignable status as long as the SCAM protocol is controlled. It continues until the status is changed by the SCAM function. When the SCAM target is separated and its Assign ID action code is received, the specified ID is set to the current and already assigned ID. The SCAM target releases all SCSI bus signals, and enters the Assigned ID status. When the SCAM target receives a Configuration Process Complete function code or the SCAM protocol has ended (if the C/D signal becomes false), the target shall release all SCSI bus signals and enter the ID Unassigned status.

Note:

The SCAM target may not recognize the Configuration Process Complete function code at the end of SCAM protocol, and may return to the SCAM Monitor status.

The SCAM target in the ID Unassigned status is the one to which no SCSI ID has been assigned both explicitly and implicitly. It does not respond to the SCSI selection of the current ID regardless of the period. The SCAM target can exit from the ID Unassigned status only when it has detected the start of SCAM protocol, except for the power-on or reset status.

Once the SCAM target has entered the ID Assigned status, it functions as a SCAM tolerant device with the already assigned ID. That is, it responds to the SCSI selection within the response time of SCAM tolerant selection but does not respond or recognize the SCAM selection.

The SCAM target can enter the Reset Delay status and allow local initialization by the reset status. The SCAM target exists this status and enters the SCAM Monitor status within a SCAM reset to SCAM selection delay.

(3) Level-2 SCAM target

Figure 1.52 shows the operations of level-2 SCAM target. Its status names are explained later. The RESET condition can terminate all operations in any status, and it forces the SCAM target to the Reset Delay status.

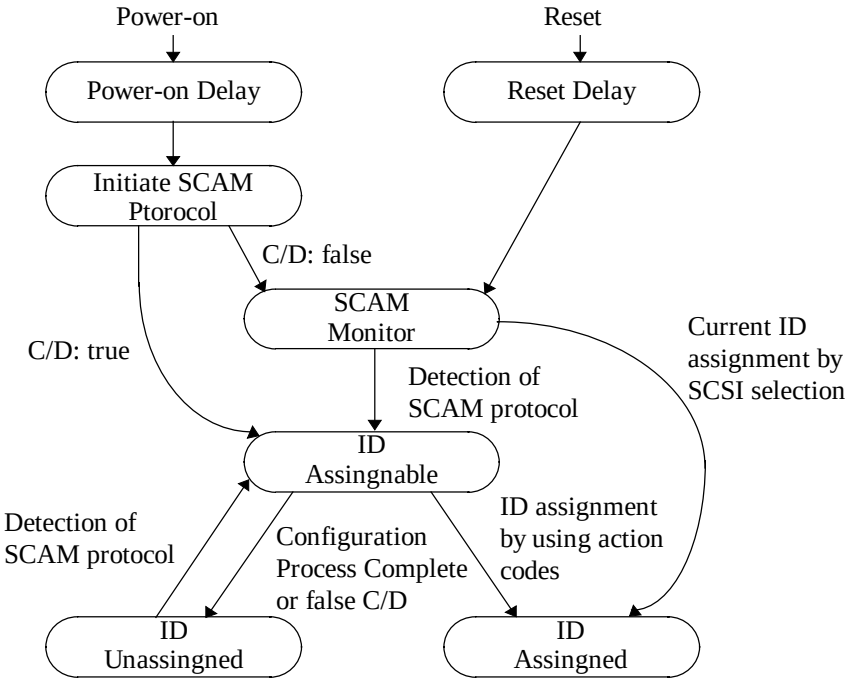


Figure 1.52 State of level-2 SCAM target

The SCAM target enters the Power-On Delay status immediately after the power-on, and allows the local initialization to start. The SCAM target shall exit this status, and enter the Initial SCAM Protocol status within a SCAM power-on to SCAM selection delay.

During Initial SCAM Protocol status, the level-2 SCAM target arbitrates the SCSI bus without using the ID and performs the SCAM selection. After SCAM selection delay, the SCAM target checks the SCSI bus and determines the C/D signal status. If the C/D signal is true, the SCAM initiator exists and its SCAM target enters in the ID Assignable status. If the C/D signal is false, the SCAM initiator does not exist and its SCAM target enters the SCAM Monitor status. Note that the level-2 SCAM target starts the SCAM protocol only once after the power-on.

During SCAM Monitor status, the SCAM target shall monitor the SCSI bus for both SCAM selection and normal SCSI selection. When the SCAM target detects the start of SCAM protocol, it shall enter the ID Assignable status. If the SELECTION phase of the current IDs of SCAM target continues to valid during at least the response delay of SCAM unassigned ID selection, this SCAM target shall respond to the selection and assert the BSY signal. The SCAM target shall implicitly enter the ID Assigned status as if its ID assignment was explicitly accepted. The assigned ID is set as the current ID, and the SCAM target functions as the SCAM tolerant device.

The SCAM target continues in the ID Assignable status as long as the SCAM protocol is controlled. It continues until the status is changed by the SCAM function. When the SCAM target is separated and its Assign ID action code is received, the specified ID is set to the current and already assigned ID. The SCAM target releases all SCSI bus signals, and enters the Assigned ID status. When the SCAM target receives a Configuration Process Complete function code or the SCAM protocol has ended (if the C/D signal becomes false), the target shall release all SCSI bus signals and enter the ID Unassigned status.

Note:

The SCAM target may not recognize the Configuration Process Complete function code at the end of SCAM protocol, and may return to the SCAM Monitor status.

The SCAM target in the ID Unassigned status is the one to which no SCSI ID has been assigned both explicitly and implicitly. It does not respond to the SCSI selection of the current ID regardless of the period. The SCAM target can exit from the ID Unassigned status only when it has detected the start of SCAM protocol, except for the power-on or reset status.

Once the SCAM target has entered the ID Assigned status, it functions as an SCAM tolerant device with the already assigned ID. That is, it responds to the SCSI selection within the response time of SCAM tolerant selection but does not respond or recognize the SCAM selection.

The SCAM target can enter the Reset Delay status and allow local initialization by the reset status. The SCAM target exists this status and enters the SCAM Monitor status within the period between SCAM reset and SCAM selection.

(4) Interconnection of various width buses

If an SCSI-3 device is mixed with an SCSI-1 or SCSI-2 device, a problem may occur. The SCSI-3 TERMPWR requirements have been expanded to support the 16-bit data bus. During this time, the SCSI-1 and SCSI-2 devices cannot supply enough TERMPWR. Also, an additional TERMPWR source (such as an SCSI-3 device) may be required.

When two buses having the different width are interconnected, the DATA BUS signal of the bus having a larger width shall be terminated with an adapter. The connector has been designed to electrically isolate the A and P shielded connectors from each other.

Two reserved lines (having A-cable contact numbers 23 and 24) and the open lines (having A-cable contact number 25) on the A cable are the TERMPWR lines (having the P-cable contact numbers 33, 34 and 35) on the P cable.

An eight-bit device connected to the single-ended P-cable shall keep open nine signals of DB(8 to 15) and DB(P1).

An eight-bit device connected to the low voltage differential P-cable shall keep open 18 signals of +DB(15 to 8), -DB(15 to 8), +DB(P1) and -DB(P1).

1.11 Ultra SCSI

1.11.1 Outline

The SCSI-3, Fast-20 Standard defines the characteristics of cables, signals, and transceivers required for 20 MB/s signal transmission. The services required to communicate with a higher layer protocol is defined by the SCSI-3 Parallel Interface Standard.

In addition, the expansion to SCSI-3 parallel interface is defined to enhance the available data transfer rate. Only the interface specifications associated with the higher data speed are included in this Standard.

1.11.2 Device connection

Connection between an single-ended transceiver and device

The maximum length of accumulated signal path between terminators shall be 3.0 m if up to four 25-pF capacitance devices are used. The maximum length of accumulated signal path between terminators shall be 1.5 m if five to eight devices that have maximum capacitance are used. When connecting nine or more devices, the specifications exceeding the minimum value defined in this manual shall be controlled. The distance between devices should be equal to each other, and the last device should locate close to the terminator as much as possible.

If the all bus elements (including cable, device interface, ambient noise, and other parameters) are controlled well to realize an environment better than the minimum required conditions, the path may be extended and more devices may be connected (see Section 1.11.3 "Single-ended I/O characteristics").

The signal path shall have the following impedance characteristics.

1) 90 +/-6 Ω for REQ and ACK signals
2) 90 +/-10 Ω for all other signals

The stub length shall not exceed 0.1 m. It shall be measured from the transceiver position toward the connection point of trunk SCSI bus. The space between devices on the trunk SCSI bus shall be at least three times larger than the stub length to prevent clustered stubs.

The ground offset voltage between logical ground terminals on any two device connectors shall be less than 50 mV.

1.11.3 Electrical characteristics of SCSI parallel interface

The Fast-20 parallel interface shall have one of the following electrical characteristics:

1) Either conductor of single-ended driver and receiver, and each signal pair shall be active, and the other conductor shall be grounded.

2) Both conductors of differential driver and receiver, and each signal pair shall be active.

The single-ended and differential transceivers cannot be used simultaneously.

(1) Single-Ended type options

a. Termination of single-ended bus signals

All SCSI bus signals are common to all devices connected to the same bus. All signal lines shall be terminated at their both ends by the terminators which are compatible to the transceivers used for SCSI devices. The end of bus shall be defined at each end point. The end point can be inside of an SCSI device.

Single-ended bus signals not defined as RESERVED, GROUND or TERMPWR shall be terminated at each bus end securely. Each signal termination shall satisfy the following requirements:

1) Each terminator shall be powered from the TERMPWR line.

2) Each terminator shall feed the current to a signal line if the terminal voltage of this signal line is 2.5 VDC or less. This current shall not exceed 24 mA if the line voltage is greater than 0.2 VDC even when all other signal lines are driven with the 4.0 VDC power.

3) Each terminator shall not feed the current to a signal line if the terminal voltage of this signal line exceeds 3.24 VDC.

4) All signal lines shall have the voltage of at least 2.5 VDC when released.

5) The terminator at each end of SCSI bus shall add a 25-pF capacitance maximum to each signal (see Section 1.11.2).

6) No terminator shall be used if it connects the 220 Ω resistance to the 5V line and the 330 Ω resistance to the ground.

Note:

These requirements shall be satisfied if any device supplies the TERMPWR.

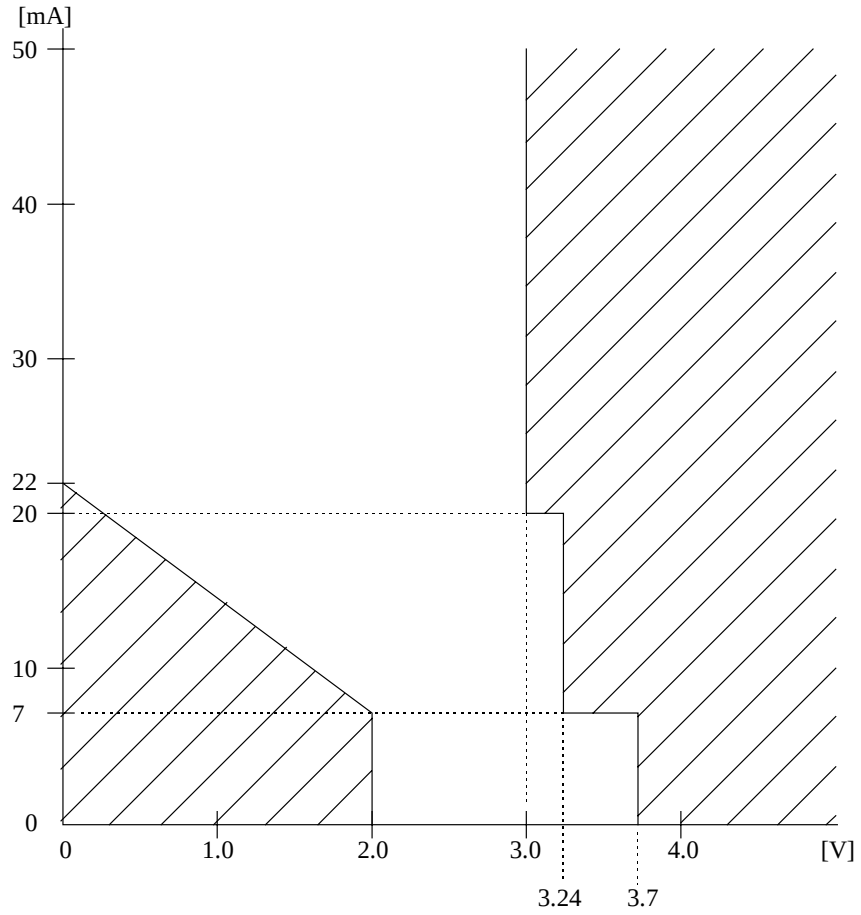
b. Single-ended output signal characteristics

An active negate driver shall be used for single-ended line signals. This driver can be in the Assert, Negate, or High-Impedance state. Each signal supplied by the SCSI device shall have the following output characteristics when measured at the connector position of SCSI device:

1) V_{OL} (Low-level output voltage) = 0.0 to 0.5 VDC if I_{OL}=48 mA (Signal assert state)

2) V_{OH} (High-level output voltage) = 2.5 to 3.7 VDC (Signal negate state)

3) The output characteristics (in signal negate state) shall be limited to allow operations in the non-shaded areas only of Figure 1.53.



Notes:

This Figure shows the operation areas allowed for DC output characteristics of active negate driver if negated. This Figure does not show the AC output characteristics. The AC output characteristics may vary depending on the other requirements including the slew rate specifications. The device load needs to be changed to measure the actual device DC characteristics. Therefore, the test circuit of Figure 1.54 cannot be used for this measurement.

Figure 1.53 Comparison of active negate current and voltage

All single-ended type drivers shall keep the high-impedance state between the power-on and power-off cycles.

The SCSI device shall satisfy the following specifications if the load capacitor (C_L) is within 15 pF +/-5% and if the unbalanced test circuit of Figure 1.54 is used for measurement.

1) t_{rise} (Rise rate) = 520 mV per ns at Max voltage (0.7 to 2.3 VDC)

2) t_{fall} (Fall rate) = 520 mV per ns at Max voltage (2.3 to 0.7 VDC)

The timing characteristics of all other signal output shall be measured using the test circuit of Figure 1.54 when the load capacitance (C_L) is within 200 pF +/-5%.

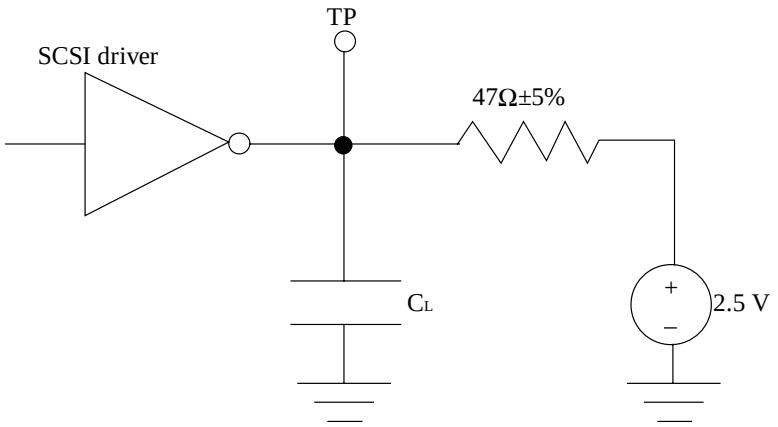


Figure 1.54 Single-ended test circuit

c. Single-ended signal input characteristics

All SCSI units (including both the receivers and disable drivers) shall meet the following electrical signal characteristics during power-on:

1) V_{IL} (Low-level input voltage) = 1.0 VDC Max (True signal)

2) V_{IH} (High-level input voltage) = 1.9 VDC Min (False signal)

3) I_{IL} (Low-level input current) = +/-20 μA if V_I=0.5 VDC

4) I_{IH} (High-level input current) = +/-20 μA if V_I=2.7 VDC

5) Minimum input hysteresis = 0.3 VDC

The transient leakage current, which may be generated during physical insertion of an SCSI device (for example, at the ESD protection circuit), shall be the exponentially decreasing current to be less than the following specifications value:

1) $I_{IH\cdot HP}$ (High-level input current peak during active insertion except for initial 10 ns) = +1.5 mA

where, V_I=2.7 VDC.

2) T_{HP} (transient current duration to 10% of peak value) = 20 μs maximum

1.12 Low-Voltage Differential

1.12.1 Ultra2-SCSI

The SPI-2, Fast-40 Standard defines the characteristics of cables, signals, and transceivers required for 40 MB/s signal transmission. The services required to communicate with a higher layer protocol is defined by the SPI-2.

In addition, the expansion to SPI-2 parallel interface is defined to enhance the available data transfer rate. Only the interface specifications associated with the higher data speed are included in this Standard.

1.12.2 Ultra-160

The technologies of the following are added since Ultra2-SCSI:

(1) DT data transfer mode (Up to maximum data transfer rate :160MB/s)
(2) Domain Validation (Write/Read Buffer Command with Echo Buffer Option)
(3) Parity CRC Available (P_CRCA) (DATA Phase CRC Protection)

These technologies are included in Ultra3-SCSI and are part of it. The name "Ultra-160" isn't in SCSI Parallel Interface – 3 (SPI-3) but is generally well known in the hard disk market. The technology "Ultra-160" enable synchronous data transfer rate of more than 80 megatransfers per second and less than or equal to a transfer rate of 160 megatransfers per second. And Ultra-160 is supported only in LVD mode.

The DT data transfer mode in detail is written in Subsection 1.6.5.2 compared ST data transfer mode.

The act of verifying that the physical layer is able to transfer test data at the negotiated speed and width between the INIT and TARG — (i.e., a quick check for physical domain validation). For example, two wide SCSI devices connected with a narrow cable will discover that the cable does not support wide transfers during this checking. These SCSI devices will then re-negotiate to narrow transfers.

A signal sourced by a target during DT DATA phases to control whether a data group field is a pad field, pCRC field, or data field. When asserted the data group field shall be pad or pCRC fields that shall not be transferred to the ULP. When negated the data group field shall be a data field that shall be transferred to the ULP.

1.12.3 Ultra-320

The new technologies of the following are added since Ultra-160 SCSI:

(1) Paced transfer mode (Up to maximum data transfer rate :320MB/s)
(2) Information unit transfer(All information transfers are performed in DT Data-In and DT Data-Out phase, except for QAS message)

These technologies are included in Ultra4-SCSI and are part of it. The name "Ultra-320" isn't in SCSI Parallel Interface - 4 (SPI-4) but is generally well known in the hard disk market. The technology "Ultra-320" enable synchronous data transfer rate of more than 160 megatransfers per second and less than or equal to a transfer rate of 320 megatransfers per second. And Ultra-320 is supported only in LVD mode.

The Pased transfer mode in detail is written in Subsection 1.6.5.3.

The Information unit trasfer in detail is written in Subsection 1.9.

1.12.4 LVD driver characteristics

The LVD driver shall provide balanced asymmetrical sources that provide current from positive supply voltage to one signal line while sinking the same current to ground from the other signal line as shown in Figure 1.55 Diagonally opposite sources operate together to produce a signal assertion or a signal negation. An assertion is produced when positive supply voltage current is sourced from source 4 to the +signal line and source 2 sinks the same current from the -signal line to ground. A negation is produced when positive supply voltage current is sourced from source 1 to the -signal line and source 3 sinks the same current from the +signal line to ground.

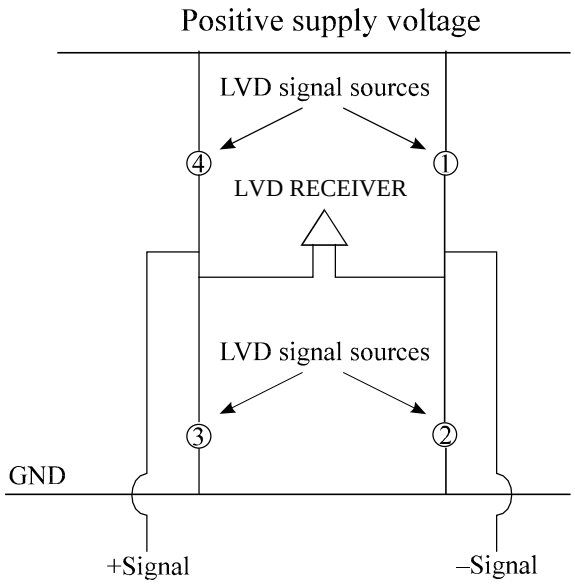


Figure 1.55 LVD transceiver architecture

Balanced transmissions occur when the changes in +SIGNAL current and the changes in the –SIGNAL current precisely cancel each other. The balance is important to reduce EMI and common mode signals. Asymmetry occurs when the intensity of the source 2 and 4 assertion pair is different from the source 1 and 3 negation pair. To compensate for the negation biasing effect of the terminators, the 2 and 4 assertion pair is stronger than the 1 and 3 negation pair.

1.12.5 LVD receiver characteristics

LVD receivers should be connected to the +signal and –signal as shown in Figure 1.56.

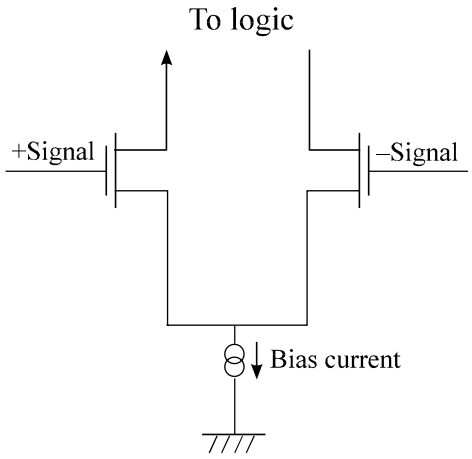


Figure 1.56 Connection to the LVD receivers

1.12.6 LVD capacitive loads

There are three components to differential SCSI bus capacitive loading: –Signal to local ground (C1), +Signal to local ground (C2), and –signal to +signal (C3) as shown in Figure 1.57. The values C1, C2, and C3 represent measurements between the indicated points and do not represent discrete capacitors. Capacitance measurements shall be made with a nominal 1MHz source with the same nominal D.C. level on the +signal and the -signal as specified in Table 1.33. The driving source from the instrumentation shall apply an A.C. signal level less than 100 mV rms.

Devices containing the enabled bus termination shall have maximum values 1.5 times the maximums listed in Table 1.33. Differential bus termination circuitry that is not part of a device shall have maximum values 0.5 times the maximums listed in Table 1.33.

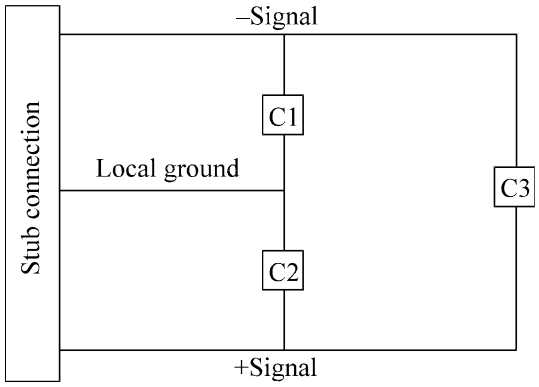


Figure 1.57 Differential SCSI bus capacitive loading

Table 1.33 Maximum capacitance

Capacitance measurement	Max.	Notes
C1(pF)	15	@V=0.7 to 1.8 VDC -Signal/GND REQ, ACK and DB(15-0,P_CRCA,P1)
C2(pF)	15	@V=0.7 to 1.8 VDC -Signal/GND REQ, ACK and DB(15-0,P_CRCA,P1)
C3(pF)	8	@V=0.7 to 1.8 VDC -Signal/GND REQ, ACK and DB(15-0,P_CRCA,P1)
C1(pF)	25	@V=0.7 to 1.8 VDC -Signal/GND all other signals
C2(pF)	25	@V=0.7 to 1.8 VDC -Signal/GND all other signals
C3(pF)	13	@V=0.7 to 1.8 VDC -Signal/GND V is the same for both signals +/- 100 mV all other siganls
|C1-C2| (pF)	1.5	REQ, ACK and DB(15-0, P_CRCA, P1)
|C1-C2| (pF)	3	All other signal
|C1 – C1(REQ)|(pF)	2	For C1is any capacitance of DB(15-0,P_CRCA,P1)
|C2 – C2(REQ)|(pF)	2	For C2is any capacitance of DB(15-0,P_CRCA,P1)
|C1 – C1(ACK)|(pF)	2	For C1is any capacitance of DB(15-0,P_CRCA,P1)
|C2 – C2(ACK)|(pF)	2	For C2is any capacitance of DB(15-0,P_CRCA,P1)

1.12.7 System level requirements for LVD SCSI drivers and receivers

The requirements for LVD SCSI drivers and receivers are based on the system level requirements stated in Table 1.34. Some of these requirements are specifically called out in other subclauses while others are derived from bus loading conditions and trade-offs between competing parameters.

Table 1.34 System level requirements

Parameter	Minimum	Maximum
V_A (except OR-tied signals) (1)	-1 V	-100 mV
V_N (except OR-tied signals) (1)	100 mV	1 V
V_A (OR-tied signals) (1)	-3.6 V	-100 mV
V_N (OR-tied signals) (1)	100 mV	125 mV
Attenuation (%) (2)		15
Loaded media impedance (ohms) (3)	85	135
Unloaded media impedance (ohms)	110	135
Terminator bias (mV)	100	125
Terminator impedance (ohms)	100	110
Device leakage (μA)	-20	20
Number of SCSI devices	2	16
Ground offset level (mV) (4)	-355	355

Note:

(1) These are the signal levels at the receiver, the system allows 60 mV crosstalk for calculating the minimum driver level.
(2) Measured from the driver to the farthest receiver.
(3) Caused by the addition of device capacitive load.
(4) This is the difference in voltage signal commons for SCSI devices on the bus.

1.13 SCSI bus fairness

(1) Fairness Model

Implementation of the SCSI bus fairness is optional.

A SCSI device determines fairness by monitoring prior arbitration attempts by other SCSI devices.

It shall put off arbitration for itself until all lower priority SCSI devices that lost previous arbitration either win a subsequent arbitration or discontinue their arbitration attempts (e.g., as in the case where the initiator aborted an outstanding command thus removing the need to re-arbitrate).

When a SCSI device does not need to arbitrate for the SCSI bus, it shall monitor the arbitration attempts of the other SCSI devices and refresh the fairness register with the SCSI IDs of any lower priority SCSI devices that lost arbitration.

Whenever a requirement for arbitration arises, a SCSI device shall first check to see if its fairness register is clear. If the fairness register is clear, this SCSI device may now participate in arbitration. If the fairness register is not clear, the SCSI device must put off arbitration until all lower priority SCSI IDs have been cleared from the fairness register.

Lower SCSI IDs are cleared as SCSI devices either win arbitration or discontinues arbitration (e.g., as a result of an ABORT TASK, an ABORT TASK SET, a CLEAR TASK SET, a TARGET RESET Message and Hard Reset).

Arbitration fairness in targets is controlled with the disconnect-reconnect mode page.

(2) Determining fairness by monitoring prior bus activity

This standard requires that the SCSI IDs of all arbitrating SCSI devices appear on the bus within a Bus Set Delay since BSY was first asserted. After this time, a SCSI device examines the bus to detect arbitrating situation.

Since the lower priority SCSI IDs begin to disappear after an Arbitration Delay from the assertion of BSY, the data bus shall be sampled after a Bus Set Delay but before an Arbitration Delay.

(3) Fairness states

A SCSI device is in one of three following fairness states.

- A SCSI device is in Fairness Wait state when it is waiting for a clear fairness register to participate in arbitration.
- A SCSI device is in the Fairness Participate state when it is participating in arbitration.
- A SCSI device is in the Fairness Idle state for all other conditions. A SCSI device should enter the fairness idle state after any reset event.

A SCSI device should implement a lockout delay to prevent devices that stop arbitrating from causing deadlock.

CHAPTER 2 SCSI MESSAGE

This chapter describes SCSI messages and their operations for controlling the operation sequence of the SCSI bus.

Note:

The IDD operates as a target device (TARG) on the SCSI bus. The IDD is referred to as the TARG in this chapter except when its clear identification is required.

2.1 Message System

The message system provides procedures for information (or message) transfer between two SCSI devices on the SCSI bus in order to control a series of bus phase sequence during command execution. The messages are transferred over the SCSI data bus in the MESSAGE OUT and MESSAGE IN phases.

2.1.1 Message format

There are three message formats are listed below. The first byte of the message is a message code in any format. (See Figure 2.1.)

- One-byte message: This consists of a message code only.
- Two-byte message: Message code is between X'20' and X'2F'. This consists of a message code and one-byte length parameter.
- Extended message: This is a message of multiple bytes length message code of X'01'.

  The Extended message code and message length are specified in the message.

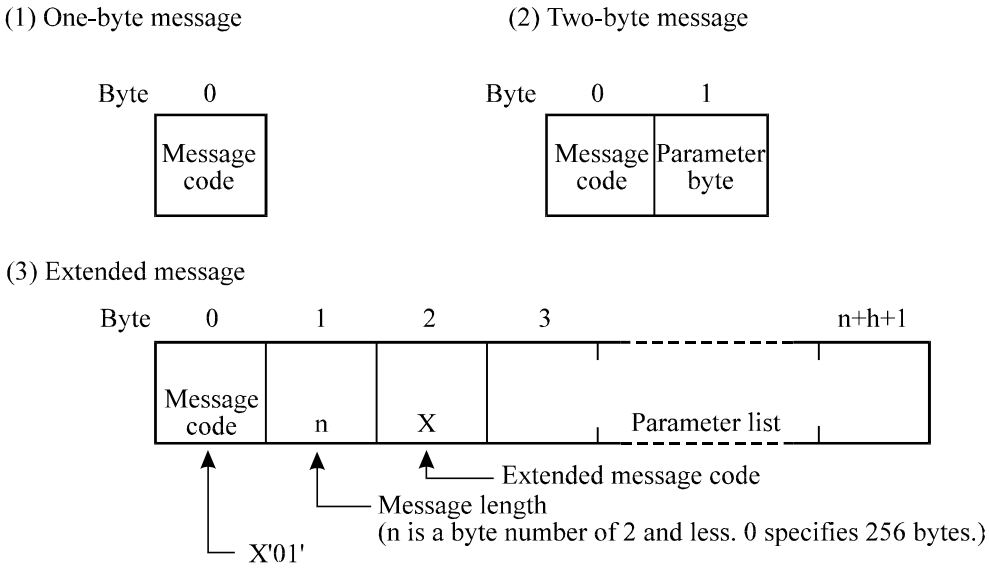


Figure 2.1 Message format

2.1.2 Message type

Message types are shown in Tables 2.1 and 2.2. Function of each message is explained in detail in Section 2.3.

Table 2.1 SCSI message

Code (hex.)	Message	Number of bytes	Transfer direction	ATN release
00	TASK COMPLETE	1	TARG→INIT	
01	EXTENDED MESSAGE (See Figure 2.1 and Table 2.2.)	n+2	TARG↔INIT	(See Table 2.2)
02	SAVE DATA POINTER	1	TARG→INIT	
03	RESTORE POINTERS	1	TARG→INIT	
04	DISCONNECT	1	TARG→INIT	
05	INITIATOR DETECTED ERROR	1	TARG←INIT	*
06	ABORT TASK SET	1	TARG←INIT	*
07	MESSAGE REJECT	1	TARG↔INIT	*
08	NO OPERATION	1	TARG←INIT	*
09	MESSAGE PARITY ERROR	1	TARG←INIT	*
0A	LINKED TASK COMPLETE	1	TARG→INIT	
0C	TARGET RESET	1	TARG←INIT	*
0D	ABORT TASK	1	TARG←INIT	*
0E	CLEAR TASK SET	1	TARG←INIT	*
12	CONTINUE TASK	1	TARG←INIT	*
13	TARGET TRANSFER DISABLE	1	TARG←INIT	*
1C	LOGICAL UNIT RESET	1	TARG←INIT	*
20	SIMPLE	2	TARG↔INIT	
21	HEAD OF QUEUE	2	TARG←INIT	
22	ORDERED	2	TARG←INIT	
23	IGNORE WIDE RESIDUE	2	TARG→INIT	
80 to FF	IDENTIFY	1	TARG↔INIT	

Note:

If a signal is identified by an asterisk (*) in the "ATN release" column, its ATN signal shall be made false at least 610 μs (Deskew Delay × 2) before the ACK signal of last byte of the message is made true by the INIT. The INIT should satisfy this requirement. However, the IDD does not force the INIT to satisfy this requirement but continues the MESSAGE OUT phase if the ATN signal is true.

Table 2.2 Extended message

Code (hex.)	Message	Number of bytes	Transfer direction	ATN release
01	SYNCHRONOUS DATA TRANSFER REQUEST	5	TARG↔INIT	*
03	WIDE DATA TRANSFER REQUEST	4	TARG↔INIT	*
04	PARALLEL PROTOCOL REQUEST	8	TARG↔INIT	*

2.1.3 Message protocol

(1) Message implement requirements

All SCSI devices shall implement at least the TASK COMPLETE message. If a logical unit number (LUN) for input and output operations is specified in the command (CDB), the minimum I/O operations required on the SCSI bus can be executed without using any message other than the TASK COMPLETE message.

Also, the SCSI device should implement the MESSAGE REJECT message against inappropriate message reception. The SCSI device must always implement the MESSAGE REJECT message if it supports any message other than the TASK COMPLETE message. In addition, the SCSI device supporting the parity check of SCSI data bus should implement the MESSAGE PARITY ERROR message.

(2) ATTENTION condition

If SCSI device supports messages other than TASK COMPLETE message, the SCSI device creates ATTENTION condition or responds to the ATTENTION condition.

To indicate that the TARG can support messages other than TASK COMPLETE message, the TARG initiates MESSAGE OUT phase in response to ATTENTION condition.

Note:

If the INIT is in the ARBITRATION phase and if it generates an ATTENTION condition, it shall assert the ATN signal before the SELECTION phase starts. If the INIT is not in the ARBITRATION phase, it shall asserts the ATN signal when sending an SEL signal.

The TARG starts the MESSAGE OUT phase in response to the ATTENTION condition immediately after the end of SELECTION phase. It shows that the TARG supports messages other than the TASK COMPLETE message.

If the TARG starts the INFORMATION TRANSFER phase (other than the MESSAGE OUT phase) when the INIT has generated an ATTENTION condition in the SELECTION phase, the INIT should negate the ATN before responding to the first ACK signal. If the ATTENTION condition is not generated during SELECTION phase, the TARG shall not send any message except for the TASK COMPLETE message to the INIT.

(3) Path establishment of I/O operation

After the SELECTION phase, the IDENTIFY, ABORT TASK SET, or TARGET RESET message must first be sent from the INIT to the TARG. The IDENTIFY message can be followed by another message such as a SYNCHRONOUS DATA TRANSFER REQUEST message.

If tagged queuing technique is used, the TASK SET message is issued immediately after the IDENTIFY message. This IDENTIFY message establishes an I/O operation path for the logical unit specified by the INIT.

After the end of RESELECTION phase, the TARG shall first send the IDENTIFY message to the INIT. This IDENTIFY message establishes an I/O operation path for the logical unit specified by the TARG. If the tagged queuing is used, the SIMPLE message is issued after the IDENTIFY message.

If the INIT has enabled the disconnect processing and if it has established an I/O operation path for the specific logical unit (by issuing the IDENTIFY message), the INIT shall set the current pointer value to the same value (the initial value) of the Saved pointer value of the logical unit. During reconnection processing (that is, when the IDENTIFY message is issued after the RESELECTION phase), the pointer is restored implicitly (and the Saved pointer value is set to the current pointer value).

2.2 SCSI Pointer

The SCSI pointer feature is required by the INIT to control the command execution on the SCSI bus. It allows multiple TARGs and logical units to process multiple commands concurrently, and allows the TARG to retry processing in bus phases.

(1) Type of pointers

The following three types of SCSI pointers have been defined:

- Command pointer: controls and manages the command (CDB) transfer.
- Data pointer: controls and manages data transfer.
- Status pointer: controls and manages the status byte transfer.

All INITs must have these three types of pointers listed above. These pointers indicate INIT memory addresses for status byte storage, data transfer, and command (CDB) fetch when viewed from the SCSI device functioning as a TARG.

The INIT needs to have one pair of current pointers and several pairs of saved pointers. The current pointers are used for the command which is being executed by the TARG currently associated with the INIT. A current pointer value is updated every time one-byte information is transferred in the INFORMATION TRANSFER phase. On the other hand, there is one pair of saved pointers for every command issued by the INIT (during its execution on the SCSI bus or disconnection). The values of the current and saved pointers are identical (initial value) when the command is issued.

(2) Pointer operation

When the TARG issues a request message or executes reconnection, the INIT saves the pointer (that is, the INIT sets the current pointer value to the Saved pointer) or restores the pointer (that is, the INIT sets the Saved pointer value to the current pointer).

Within the Saved pointer, the command pointer and status pointer always have their initial value of that command. The command pointer points to the first byte position of the CDB (command), and the status pointer points to the storage position of status byte in that command. While in the Saved pointer, the data pointer points to the beginning of data area of the command when the command execution has started. These values are held until the TARG issues a SAVE DATA POINTER message to the INIT. When the INIT receives this SAVE DATA POINTER message, the INIT stores the current data pointer value in the saved data pointer area.

The TARG can restore the pointers by sending the RESTORE POINTERS message to the INIT. When the INIT receives this RESTORE POINTERS message, it stores pointer values of the saved pointer in the corresponding current pointer.

If the INIT receives an IDENTIFY message after the RESELECTION phase, the INIT restores the pointers in the similar way as when it has received the RESTORE POINTERS message.

If a command is in the disconnect state, the INIT saves only the saved pointer value of the command. Therefore, if the command disconnect is expected during data transfer, the TARG shall save the current data pointer values by issuing the SAVE DATA POINTER message before issuing the DISCONNECT message.

Note:

As the TARG may set any pointer value before starting disconnect processing or command termination, the pointer value of the INIT may or may not point to the byte position of the data recently transferred over the SCSI bus.

Figure 2.2 shows the SCSI pointer configuration. It indicates the execution of the command (CDB_0) after the INIT was connected with TARG#0 and LUN#0. Therefore, the current pointer keeps each pointer value to execute the command (CDB_0). The initial values for the command, data, and status pointers for this command are X_0, Y_0, and Z_0.

The current pointer values are updated to (X_0 + c) and (Y_0 + d) by fetching the command (CDB_0) and executing the data transfer. The saved pointer values except for the data pointer keep the initial values (X_0, Z_0) until the command execution ends. The saved data pointer value keeps the initial value at the command issuance, (Y_0), or the current pointer value at the time the pointer saving operation was performed by the TARG specification, (Y_0 + dn). These saved pointer values can be restored into the current pointer by a RESTORE POINTERS message when the TARG retries the command.

Also, the pointers to the commands (CDB_1, CDB_m) which are in operation with other logical units are stored at the corresponding positions (1, m) in the saved pointer group. They are fetched and restored as the current pointers when the commands are reconnected.

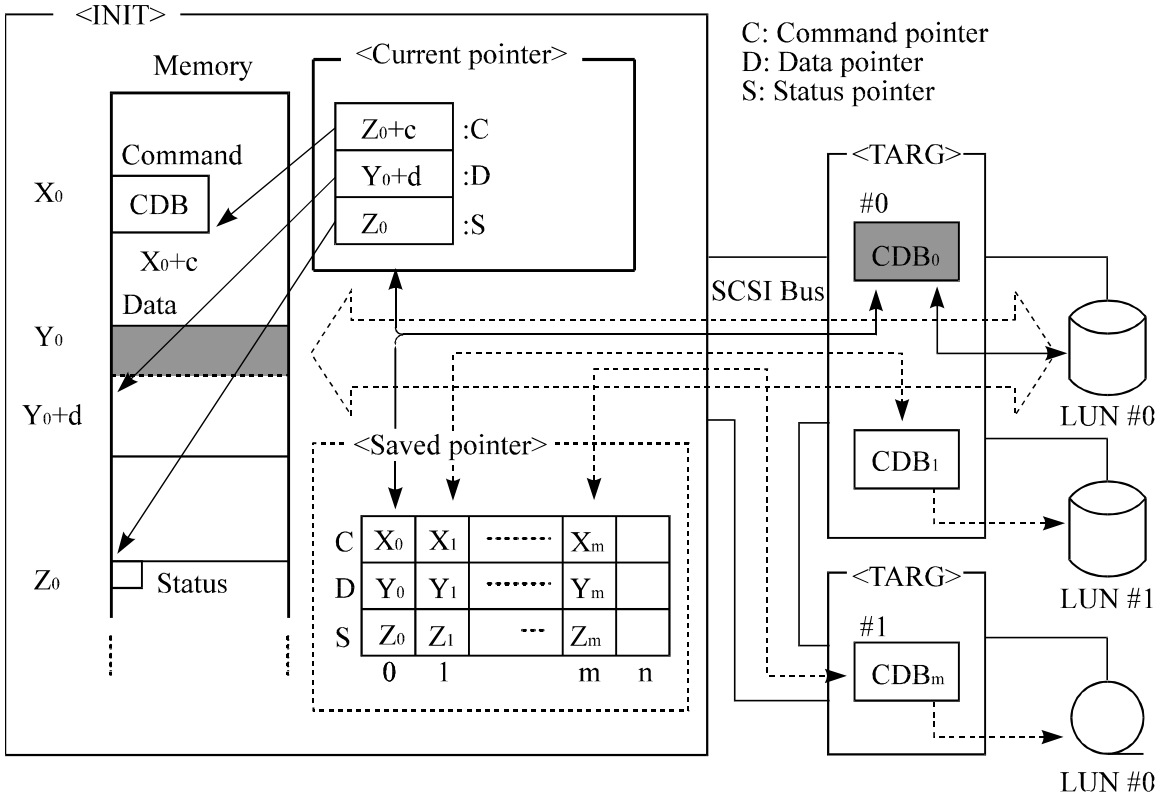


Figure 2.2 SCSI pointer configuration

2.3 Message Explanation

This section explains the function of each message. The following symbols are used for message identification.

Symbols:

(I→T): The message which can be sent from the INIT to the TARG only.
(T→I): The message which can be sent from the TARG to the INIT only.
(I↔T): The message which can be sent between the INIT and TARG in any direction.

2.3.1 TASK COMPLETE message: X'00'(T→I)

The TASK COMPLETE message indicates that an unlinked command or a series of linked commands have been executed and that a valid status information has been posted to the INIT.

This message notifies the INIT the validity of status information but the command may or may not have been executed normally. The command completion status is indicated by the status byte which is sent in the STATUS phase prior to this message.

When the TARG sends the status byte to the INIT, the TARG always sends this message after the STATUS phase even if the normal command (CDB) transfer has failed (due to a parity error of SCSI data bus in MESSAGE OUT or COMMAND phase).

When the TARG completes normal message transfer, it enters the BUS FREE phase. The TARG determines that the message transfer has completed normally if the ATN signal is false when the ACK signal becomes false.

2.3.2 SAVE DATA POINTER message: X'02'(T→I)

The SAVE DATA POINTER message requests the INIT to save the current data pointer. When receiving this message, the INIT stores the value of current data pointer into the Saved pointer for the currently connected LUN. For the disconnection message, see Section 2.3.3.

2.3.3 RESTORE POINTERS message: X'03' (T→1)

The RESTORE POINTERS message requests the INIT to restore the current SCSI pointers. If this message is received, the INIT restores the value of Current SCSI pointers with the value of the Saved pointers for the corresponding I/O process. For the SCSI Pointers, see Section 2.2.

2.3.4 DISCONNECT message: X'04' (T→I)

The DISCONNECT message informs to the INIT that the TARG disconnects the SCSI bus temporary. After the TARG has sent this message, it enters the BUS FREE phase and the disconnection completes. The TARG determines that the message transfer has completed normally if the ATN signal is false when the ACK signal becomes false.

The TARG continues command processing by itself, and reconnects the INIT when necessary (by reconnect processing) to continue command execution on the SCSI bus.

This message cannot request the INIT for saving of the current data pointer.

Note:

To start disconnect processing during data transfer, the TARG must send the SAVE DATA POINTER message for saving of data pointer before sending this message. This is required even if all bytes of data specified by the command have already been transferred.

2.3.5 INITIATOR DETECTED ERROR message: X'05'(I→T)

The INITIATOR DETECTED ERROR message informs to the TARG that the INIT has detected an error which allows command retry by the TARG. The error cause may be associated with the SCSI bus operations or INIT internal operations.

If this message is posted, the current pointer value is unreliable. Section 3.1 explains the details of recovery processing when the IDD receives this message.

2.3.6 ABORT TASK SET message: X'06' (I→T)

The ABORT TASK SET message requests the TARG to clear the currently executing or queued I/O operations. When the TARG receives this message, it immediately performs the following (regardless of the ATN signal status).

If the LUN has been determined prior to this message, the TARG clears all of the currently executing or queued I/O operations which have been initiated to the specified logical unit by the source INIT of this message, and enters the BUS FREE phase. All of the hold data and status information, or the sense data of the logical unit and INIT are cleared. If the I/O operations are cleared by this message, their status byte and end messages are not sent to the INIT. This message does not affect on the I/O operations initiated by another INIT.

If the LUN has not been determined prior to this message, the TARG enters the BUS FREE phase without any operation. This message does not affect on the currently executing or queued I/O operations.

If this message is issued to the LUN which does not have the information about the currently executing or queued I/O operations or sense data status, the TARG does not generate an error condition but enters the BUS FREE phase.

To clear the disconnected I/O operations, the INIT can send the IDENTIFY and the ABORT TASK SET messages in succession immediately after the TARG selection (in SELECTION phase).

Note:

The TARGET RESET, CLEAR TASK SET, ABORT TASK SET, and ABORT TASK messages can clear one or more I/O operations before they terminate normally.

- TARGET RESET message: Clear all I/O operations of all INITs existing on all LUNs of the TARG.

- CLEAR TASK SET message: Clear all I/O operations of all INITs existing on a specific LUN.

- ABORT TASK SET message: Clear all I/O operations of a specific INIT existing on a specific LUN.

- ABORT TASK message: Clear a single I/O operation only.

2.3.7 MESSAGE REJECT message: X'07'(I↔T)

The MESSAGE REJECT message indicates that the recently received message or message bytes are inappropriate or has not been implemented.

When the INIT sends this message, to allow the TARG to identify the rejected message, it shall assert the ATN signal before negating the ACK signal associated when the TARG received a message to be rejected in the MESSAGE IN phase. If the TARG receives this message anytime except when it responds to the ATN signal, it shall reject this message.

When the TARG sends this message, the TARG shall enter the MESSAGE IN phase and send this message after negating the ACK signal associated with the rejected message if it is received in the MESSAGE OUT phase. This is required to allow the INIT to identify the rejected message.

Section 3.1 explains the IDD operation details when the INIT returns this message in response to the message sent by the IDD.

2.3.8 NO OPERATION message: X'08' (I→T)

The NO OPERATION message does not result in any operation. If the INIT has no valid messages which can be sent in response to a send request from the TARG (in MESSAGE OUT phase), the INIT sends this message to the TARG.

2.3.9 MESSAGE PARITY ERROR message: X'09' (I→T)

The MESSAGE PARITY ERROR message notifies the TARG that a parity error has been detected in the message byte recently received by the INIT.

To allow the TARG to identify the message having the parity error, the INIT shall assert the ATN signal, generate an ATTENTION condition, and send this message first. Then, the INIT shall negate the ACK signal associated with the message which indicates a parity error in the MESSAGE IN phase.

Section 3.1 explains the IDD operation details when the INIT returns this message in response to the message sent by the IDD.

2.3.10 LINKED TASK COMPLETE message: X'0A'(T→I)

The LINKED TASK COMPLETE message indicates that the link command (with flag bit 0) has been executed normally and that the valid status byte has been posted to the INIT. When the INIT receives this message, it shall update both the current pointer and Saved pointer to the initial values of the next linked command.

2.3.11 TARGET RESET message: X'0C' (I→T)

The TARGET RESET message requests the TARG to clear all of the currently executing or queued I/O operations (or commands). The TARG shall clear both the I/O operations initiated by the INIT of this message source and I/O operations of all INITs. When the TARG receives this message, it shall enter the BUS FREE phase immediately (regardless of the subsequent ATN signal status).

2.3.12 ABORT TASK message: X'0D' (I→T)

When the TARG receives this message normally, it enters the BUS FREE phase. The TARG clears the current I/O operation and stops its current execution. The medium contents may have been modified before the execution is aborted. In either case, the hold status or data of the I/O operation is cleared. No status or end message is sent to the INIT. This message does not affect on the held status, data, and commands of the I/O operations which are being executed or queued by another unit. Also, this message does not abort another I/O operation which is queued in the INIT of this message source.

The system environment and conditions previously established by the MODE SELECT parameter are not changed by this message.

2.3.13 CLEAR TASK SET message: X'0E'(I→T)

When the TARG receives the CLEAR TASK SET message, it enters the BUS FREE phase. The TARG operates in the similar way as when it receives a series of ABORT TASK SET messages from each INIT. This message clears all I/O operations currently being executed or queued in the specified logical unit. The medium contents may have been modified before the execution is aborted. All status and data held in all INITs are cleared. No status or message is sent to the INIT. If the I/O operations of INITs, which differ from the INIT of this message source, are cleared, a UNIT ATTENTION condition is generated for those INITs. When the UNIT ATTENTION condition is reported, the Sense data indicates the COMMANDS CLEARED BY ANOTHER INITIATOR [=2F-00].

The system environment and conditions previously established by the MODE SELECT parameter are not changed by this message.

2.3.14 CONTINUE TASK message: X'12' (I→T)

The CONTINUE TASK message is sent from the INIT to the TARG to reconnect to a task. This message shall be sent as one of the messages within the consecutive message out phases sent after the IDENTIFY message.

Thus the messages within the consecutive message out phases following a selection phase consists of the IDENTIFY, task attribute (if any), and CONTINUE TASK messages.

The purpose of the CONTINUE TASK message is to distinguish a valid INIT attempt at a reconnection phase from an incorrect initiator reconnection phase.

If the TARG expects a significant delay before it will be ready to continue processing the reconnected task, it may attempt to free the SCSI bus by sending a DISCONNECT message to the INIT. The INIT may reject the disconnection attempt by responding with MESSAGE REJECT message.

If the CONTINUE TASK message occurs on an initial connection then the TARG shall generate a bus free phase.

If the CONTINUE TASK message occurs on a subsequent connection then the TARG may either treat this as a dynamic head-of-queue request or it may reject the message with a MESSAGE REJECT message.

An INIT that gets rejected should set the attention flag to one and send an ABORT TASK message on the resulting message out phase. Otherwise, the TARG may treat the connection as an overlapped command.

The INIT should avoid sending this message to the TARG that have not implemented this message. Such the TARG may not respond as described in this section. An application client can determine whether a device server implements this message by examining the TRANDIS bit in the standard INQUIRY data. The application client shall inform the INIT to use the CONTINUE TASK message by issuing a TARGET TRANSFER DISABLE link control function in the send SCSI command phase.

The IDD does not support this message.

2.3.15 TARGET TRANSFER DISABLE message : X'13' (I→T)

The TARGET TRANSFER DISABLE message is sent from an INIT to a TARG to request that subsequent reconnections for data transfer be done by the INIT instead of the TARG. The TARG might reconnect for other purposes, but shall not generate any data in phase or data out phase after a TARG reconnection. SCSI devices that implement this message shall also implement the CONTINUE TASK message.

This message shall be sent as the last message of the series of consecutive message out phase of an initial connection. The TARG may continue the task, including any data out phase on the initial connection, until the TARG would normally disconnect, but the TARG shall not.

Reconnect to transfer data. That is, the TARG shall not generate a data in phase on the initial connection and the TARG shall not generate any data in or data out phases on any subsequent TARG reconnection for the task.

When the TARG is ready to transfer data for a disconnected task for which a TARGET TRANSFER DISABLE message has been sent, the TARG shall reconnect to the INIT for the task (via a reselection phase and consecutive message in phases containing an IDENTIFY message, and an optional SIMPLE message), send a DISCONNECT message, and, if the INIT does not respond with a MESSAGE REJECT message, generate a bus free phase. This connection serves to notify the INIT that the task is ready for data transfer. If the INIT rejects the DISCONNECT message, the TARG may generate a data in or data out phase; otherwise, the INIT may reconnect to the task as described in the CONTINUE TASK message to perform the data transfer.

INITs should avoid sending the TARGET TRANSFER DISABLE message to the TARG that have not implemented this message. Such the TARG may not respond as described in this section. An application client can determine whether a device server implements this message by examining the (TRANDIS) bit in the standard INQUIRY data.

The application client shall inform the INIT to use the CONTINE TASK message by issuing a TARGET TRANSFER DISABLE link control function in the send SCSI command phase.

The IDD does not support this message.

2.3.16 LOGICAL UNIT RESET message : X'1C' (I→T)

When the TARG receives this message normally, it enters the BUS FREE phase.

In case the I_T_L_x nexus has been established with LUN=0, TARG clears all the tasks in the logical unit and generates UNIT ATTENTION condition for all INITs. Receipt of this message has no effect on the MODE SELECT parameters and negotiated transfer agreements.

In case the I_T_L_x nexus has been established with non zero LUN or I_T nexus has been established, TARG clears the task that is currently executed. In this case, there is no effect on the other tasks.

2.3.17 Task attribute messages

Bit / Byte	7	6	5	4	3	2	1	0
0	Message Code (X'20', X'21', or X'22')							
1	TAG (X'00'- X'FF')							

The task attribute messages define a queue tag of I/O operation. The TAG field is an unsigned eight-bit integer to be assigned by the INIT when it issues a command.

When the INIT issues a command using a tagged queuing, the INIT sends the appropriate task attribute messages immediately after the IDENTIFY message during the same MESSAGE OUT phase in order to set the queue tag for the I/O operation. If the task attribute messages are not sent, the I/O operation is treated as an untagged command.

If the TARG reconnects to the INIT to continue a tagged I/O operation, the TARG sends the SIMPLE message immediately after the IDENTIFY message in the reconnection sequence of the same MESSAGE IN phase.

(1) SIMPLE message: X'20'(I↔T)

The SIMPLE message specifies that the task be placed in that logical unit's queue. The order of execution is determined by the IDD.

(2) HEAD OF QUEUE message: X'21'(I→T)

The HEAD OF QUEUE message specifies that the task be placed first in that logical unit's command queue. A subsequent task received with a HEAD OF QUEUE message is placed at the head of the command queue for execution in last-in, first-out order.

(3) ORDERED message: X'22'(I→T)

The ORDERED message specifies that the task be placed in that logical unit's command queue for execution in the order received. All queued tasks for the logical unit received prior to this I/O process are executed before this task is executed. All queued tasks received after this task is executed after this task, except for tasks received with a HEAD OF QUEUE message.

2.3.18 IGNORE WIDE RESIDUE message: X'23' (T→I)

Byte \ Bit	7	6	5	4	3	2	1	0
0	Message Code (X'23')							
1	Number of bytes to IGNORE (X'01')							

This message the number of bytes of invalid data is notified from TARG to INIT when not coming up to the width of the data bus which the number of bytes of data which transfers to INIT by the last REQ/ACK handshake of the DATA IN phase and the REQB/ACKB handshake uses in the place where the wide data transfer is executed.

When it is necessary to send this message, TARG executes the MESSAGE IN phase without fail immediately after the end of the DATA IN phase, and transmits this message first.

All the numbers of bytes of data transferred at the end become effective in the place where this message is not sent.

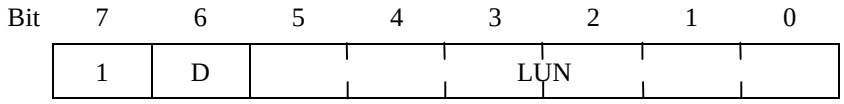
The number of bytes of data which transferred at the end does not come up to the width of the data bus in the place where DISCONNECT is done before forwarding all the data specified by the task (DATA IN phase) ends TARG transmits this message before the SAVE DATA POINTER message.

INIT renews the current data pointer according to the invalid number of data bytes notified by this message.

Note:

The number of effective bytes of data which transfers by the data phase and boundary need not use this message at the data out phase because TARG controls.

2.3.19 IDENTIFY message: X'80' to X'FF' (I↔T)



This message specifies the logical unit number (LUN) for the device (logical unit) under the TARG and establishes an I/O operation path between the INIT, TARG, and logical unit.

a. Bit 6: Disconnect Privilege (D)

Only the INIT can set this bit to 1. When this bit is 1, it indicates that the INIT permits the TARG to execute disconnection processing. When this bit is 0, the TARG must not execute disconnection operation. When the TARG sends this message, this bit must be 0.

b. Bits 5 to 0: LUN

These bits specify the logical unit number (LUN) for the device.

Note:

The LUN of the IDD is fixed to #0.

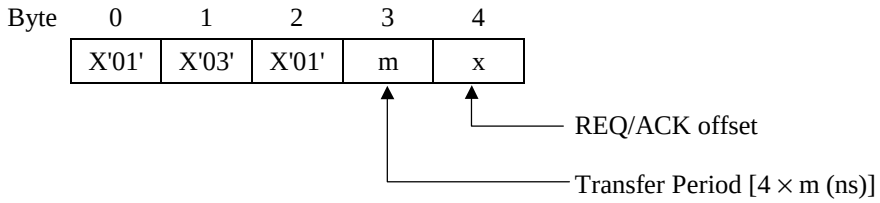
c. Function of message

After the SELECTION phase has completed, the INIT usually sends the IDENTIFY message to the TARG as the first message; this message specifies a logical unit for I/O operations. Also, after the RESELECTION phase has completed, the TARG shall send the IDENTIFY message to the INIT as the first message to inform the logical unit to be reconnected.

When an I/O operation path is established between the INIT and the TARG within a single SELECTION or RESELECTION sequence, only a single LUN can be specified. The second IDENTIFY message specifying a new LUN must not be issued until the SCSI bus is released (that is, until a BUS FREE phase is generated). The INIT can send the IDENTIFY message two or more times during a single I/O operation. In such case, value of bit 6 (Disconnect Privilege) can be changed in the second and subsequent IDENTIFY messages. However, the same LUN as specified by the first IDENTIFY message shall be specified in bits 5 to 0 (LUN).

If the INIT receives this message in the reconnection sequence, the INIT shall save the Saved pointer value of the specified LUN in the current pointer before completing the current message transfer phase (or before negating the ACK signal).

2.3.20 SYNCHRONOUS DATA TRANSFER REQUEST message (I↔T)



The synchronous data transfer parameters are defined by exchange of the SYNCHRONOUS DATA TRANSFER REQUEST message between two SCSI devices.

When a SCSI device having the synchronous transfer functions is first connected to another SCSI device after its power-on, a RESET condition (a hardware reset), or after reception of TARGET RESET message, these two devices exchange the SYNCHRONOUS DATA TRANSFER REQUEST message by each other and determine the synchronous data transfer.

Each SCSI device must always respond to this message which is issued by another SCSI device. (The SCSI devices can exchange this message to select or change the data transfer mode any time other than the first connection.)

(1) Data transfer mode parameter

Two SCSI devices exchange the SYNCHRONOUS DATA TRANSFER REQUEST message and determine the Transfer Period and REQ/ACK Offset allowance to be set during data transfer between them. These values apply to all logical units (LUNs) assigned to the two SCSI devices.

The Transfer Period is the minimum repeat cycle of REQ and ACK pulses which are allowed for data reception by SCSI devices. (It is the minimum time between the leading edge of an REQ pulse and the leading edge of the next REQ pulse, or between the leading edge of an ACK pulse and the leading edge of the next ACK pulse.)

The REQ/ACK Offset is the maximum number of REQ pulses (an offset) which the TARG can send before receiving an ACK response (the leading edge of ACK signal) from the INIT. This offset must be set to the enough value not to cause an overflow of data receive buffer and offset counter. When the REQ/ACK Offset is X'00', data is transferred in the asynchronous transfer mode. When it is X'FF', this offset is unlimited.

The SCSI device that sends the SYNCHRONOUS DATA TRANSFER REQUEST message at first sends this message with specifying the Transfer Period and REQ/ACK Offset values within the appropriate range so that the SCSI device itself can receive data normally. The SCSI device that received the SYNCHRONOUS DATA TRANSFER REQUEST message returns the SYNCHRONOUS DATA TRANSFER REQUEST message with setting same Transfer Period and REQ/ACK Offset values as received ones if it can receive data using specified parameters. If the SCSI device requires a larger Transfer Period or a smaller REQ/ACK Offset to receive data correctly, it sets the appropriate values (which can satisfy the SCSI device requirements) in the SYNCHRONOUS DATA TRANSFER REQUEST message and returns it to the sender unit.

When a SCSI device executes data transfer, it must not send REQ or ACK pulses exceeding the parameter limits which have been set by the two SCSI devices by exchange of the SYNCHRONOUS DATA TRANSFER REQUEST message. However, the SCSI device can transfer data using a larger Transfer Period or a smaller REQ/ACK Offset.

After normal exchange of the SYNCHRONOUS DATA TRANSFER REQUEST message, the two SCSI devices shall set the data transfer mode depending on the response (the returned message) by the SCSI device which has first received this message. Table 2.3 defines the data transfer mode to be selected.

Table 2.3 Definition of data transfer mode by message exchange

Responded message	Data transfer mode
SYNCHRONOUS DATA TRANSFER REQUEST REQ/ACK Offset ≥ 1	Synchronous mode: Each SCSI device executes data transfer using the Transfer Period value equal to or greater than the specified value and REQ/ACK Offset value equal to or smaller than the specified value specified in the SYNCHRONOUS DATA TRANSFER REQUEST message from the opposite SCSI device.
SYNCHRONOUS DATA TRANSFER REQUEST REQ/ACK Offset =0	Asynchronous mode
MESSAGE REJECT	Asynchronous mode

(2) Procedures of the message exchange initiated by the INIT

If the INIT has recognized the synchronous data transfer to be set, it asserts the ATN signal that is, generating an ATTENTION condition for message exchange, and requests the TARG to receive the SYNCHRONOUS DATA TRANSFER REQUEST message.

After the MESSAGE OUT phase has completed normally, the TARG shall return the SYNCHRONOUS DATA TRANSFER REQUEST message or the MESSAGE REJECT message to the INIT. If the ACK signal is still true after the TARG has received the SYNCHRONOUS DATA TRANSFER REQUEST message, the TARG can cancel the MESSAGE OUT phase and can enter the MESSAGE IN phase to return the message. If the TARG cannot return the message, the two SCSI devices shall select the asynchronous data transfer mode between them.

When the INIT sends the MESSAGE REJECT message as the first byte of the MESSAGE OUT phase which follows the MESSAGE IN phase, this negotiation is regarded as a failure and the mode setting for synchronous transfer between the INIT and the TARG must be set to the asynchronous mode. This event occurs even if the TARG returns the SYNCHRONOUS DATA TRANSFER REQUEST message with specifying 1 or more to the REQ/ACK Offset value.

If the INIT sends the MESSAGE PARITY ERROR message or the INITIATOR DETECTED ERROR message against the TARG's SYNCHRONOUS DATA TRANSFER REQUEST message, the IDD recognizes that there was a parity error in the previous MESSAGE IN phase. Then, the IDD performs the error recovery procedure based on the SCSI Bus protocol for the erroneous

phase up to 3 times. If the retry fails, this negotiation is regarded as a failure. The mode setting for synchronous transfer between the INIT and the TARG must be set to the asynchronous mode.

(3) Procedures of the message exchange initiated by the TARG

If the TARG has recognized the synchronous data transfer to be set and if the synchronous data transfer request is enabled by the CHANGE DEFINITION command, the TARG sends the SYNCHRONOUS DATA TRANSFER REQUEST message to the INIT. The INIT shall return the SYNCHRONOUS DATA TRANSFER REQUEST or MESSAGE REJECT message by asserting the ATN signal before negating the ACK signal of the last byte of SYNCHRONOUS DATA TRANSFER REQUEST message sent from the TARG. If the INIT cannot respond to this message, the two SCSI devices shall select the asynchronous data transfer mode between them.

The INIT and the TARG shall continue the synchronous data transfer even if the INIT has responded with the SYNCHRONOUS DATA TRANSFER REQUEST message. This synchronous transfer mode shall be continued until the MESSAGE OUT phase is terminated normally by transition of TARG to the INFORMATION TRANSFER phase (it indicates that no parity error has been detected). If the TARG fails to receive the response by the INIT normally after the specified number of retries, the TARG shall negate the BSY signal and shall enter the BUS FREE phase immediately without executing another INFORMATION TRANSFER phase. The INIT shall consider it as the unsuccessful message exchange and the two SCSI devices shall select the asynchronous data transfer mode between them.

If the TARG enters the MESSAGE IN phase immediately after the INIT has responded with the SYNCHRONOUS DATA TRANSFER REQUEST message, and if the TARG first sends the MESSAGE REJECT message to the INIT, the INIT shall consider it as the unsuccessful selection of synchronous data transfer. The two SCSI devices shall select the asynchronous data transfer mode between them.

If the ATN signal is still true when the message is returned by the INIT in MESSAGE OUT phase, if the TARG has normally received multiple messages in succession, and if the TARG receives the ABORT TASK SET message after the SYNCHRONOUS DATA TRANSFER REQUEST message, the TARG shall complete to process the SYNCHRONOUS DATA TRANSFER REQUEST message and validate the transfer mode selection. Then, the TARG shall execute the ABORT TASK SET message. If the TARG receives the ABORT TASK SET message before receiving the SYNCHRONOUS DATA TRANSFER REQUEST message, the two SCSI devices shall select the asynchronous data transfer mode between them.

(4) Valid cycle for the data transfer mode

After the exchange of SYNCHRONOUS DATA TRANSFER REQUEST message, the selected data transfer mode and the synchronous data transfer parameters shall be kept valid on these SCSI devices until when:

- A TARGET RESET message is received.
- A RESET condition (a hardware reset) occurs.
- The data transfer mode or parameter is changed between the two SCSI devices.
- Power turned off
- Reception of the WIDE DATA TRANSFER REQUEST message
- Change in the transceiver mode (e.g., LVD mode to SE mode).

The default data transfer mode between SCSI devices is asynchronous data transfer. The asynchronous data transfer mode shall be selected when the power supply is turned on, a TARGET RESET message is received, a RESET condition occurs, or a WIDE DATA TRANSFER REQUEST message is received.

If the synchronous transfer mode has been selected between SCSI devices and if it is changed to the asynchronous transfer mode for some reasons (such as the TARGET RESET message from another INIT) that the remote SCSI device cannot detect, the local SCSI unit shall send the SYNCHRONOUS DATA TRANSFER REQUEST message to select the transfer mode again or exchange the message for mode change. Then, the local SCSI device shall start data transfer.

By considering the system performance affected by the message exchange overhead, avoid to select the data transfer mode in every SELECTION sequence.

(5) Synchronous mode transfer function of IDD

a. Mode setup

When the TARG tries to control whether the IDD starts the negotiation if necessary, it can specify using the CHANGE DEFINITION command.

Table 2.4 Synchronous mode data transfer request setting

SDTR bit	Operation
"0"	Even if the IDD recognizes that the synchronous mode transfer and wide mode transfer settings are necessary, the IDD does not send the SYNCHRONOUS DATA TRANSFER REQUEST message. However, when the INIT sends the SYNCHRONOUS DATA TRANSFER REQUEST message, the IDD responds to the message correctly.
"1"	When the IDD recognizes that the synchronous mode transfer setting is necessary, the IDD sends the SYNCHRONOUS DATA TRANSFER REQUEST message after completing the COMMAND phase.

Refer to Section 3.1.4 in SCSI Logical Specifications for details of setting method.

b. Transfer mode definition

(a) Default transfer mode

The default transfer mode is selected automatically when the power supply is turned on, a RESET condition occurs, or the TARGET RESET message is received (initial state). This mode is kept for each INIT individually. When an SCSI device executes the first command, it exchanges the SYNCHRONOUS DATA TRANSFER REQUEST message with others. If this message exchange is successful, the synchronous transfer mode is selected between the two SCSI devices. If unsuccessful, the asynchronous transfer mode is selected between them.

(b) Transfer mode establishment

The default transfer mode is released, and the synchronous transfer mode or the asynchronous transfer mode is selected by the exchange of SYNCHRONOUS DATA TRANSFER REQUEST message.

This mode is kept for each INIT individually and data transfer mode and synchronous mode parameters of each INIT differ each other. Data is transferred in the transfer mode selected between the INIT based on the SCSI ID of the INIT which is identified in the SELECTION phase.

If the INIT is in this state, the IDD does not send the SYNCHRONOUS DATA TRANSFER REQUEST message to request for reselection of the transfer mode or changing the synchronous transfer mode parameters. However, if the INIT returns the SYNCHRONOUS DATA TRANSFER REQUEST message again, the IDD responds to it as described later and it selects the data transfer mode again or sets the synchronous data transfer parameters again.

If the retry fails in the MESSAGE IN or MESSAGE OUT phase when the SYNCHRONOUS DATA TRANSFER REQUEST message is exchanged, or if the transfer mode selection sequence has failed, the transfer mode between the INIT moves to the default transfer mode.

(c) Transfer mode when the SCSI ID is not defined for INITs

Even if the SCSI ID of the INIT is not posted in the SELECTION phase (if a single INIT is used and if it does not use the RESELECTION phase), the message can be exchanged and the data transfer mode can be selected between the IDD and the INIT. In this case, the IDD sets a unique data transfer mode for the INIT which has the undefined SCSI ID. If the system dynamically uses two types of SELECTION phase (where the SCSI ID of the INIT is posted and it is not posted), the transfer mode must be selected for each data transmission.

c. Transfer mode setup from INIT to IDD

Table 2.5 shows the IDD response to the first SYNCHRONOUS DATA TRANSFER REQUEST message sent from the INIT. Also, this table lists the data transfer modes set between the INIT and IDD by the response.

The INIT can send the SYNCHRONOUS DATA TRANSFER REQUEST message anytime. However, the IDD shall send this message to the INIT for selection of synchronous data transfer mode if the INIT has failed to send the SYNCHRONOUS DATA TRANSFER REQUEST message by the end of COMMAND phase. It is required when the IDD still maintains the default transfer mode to the INIT and when the synchronous transfer request is enabled by the CHANGE DEFINITION command (see Paragraph "d").

Table 2.5 Transfer mode setup request from INIT to IDD

(SDTR: SYNCHRONOUS DATA TRANSFER REQUEST message)

Message from INIT			IDD Response	Transfer mode to be defined
S D T R	REQ/ACK Offset	X'00'	SDTR REQ/ACK Offset = 0	Asynchronous mode
		X'01' : X'7F'	SDTR REQ/ACK Offset =Specified value by INIT	Synchronous mode REQ/ACK offset ≤ Specified value by INIT
		X'80' :	SDTR REQ/ACK Offset = X'7F'	Synchronous mode REQ/ACK offset ≤ 127
	Transfer Period	X'00' : X'0A'(25ns)	SDTR Transfer Period = X'0A'	Synchronous mode (40.0 MB/s max.) 8-bit mode (80.0 MB/s max.) 16-bit mode REQ Period ≥ 25 ns ACK Period ≥ 25 ns Notice: Only LVD type
		X'0B' (37.5 ns)	SDTR Transfer Period = X'0B'	Synchronous mode (20.0 MB/s max.) 8-bit mode (40.0 MB/s max.) 16-bit mode REQ Period ≥ 50.0 ns ACK Period ≥ 50.0 ns Notice: Only LVD type
		X'0C'(50 ns)	SDTR Transfer Period = X'0C'	Synchronous mode (20.0 MB/s max.) 8-bit mode (40.0 MB/s max.) 16-bit mode REQ Period ≥ 50 ns ACK Period ≥50 ns
		X'0D' : X'12' (72 ns)	SDTR Transfer Period = X'11'	Synchronous mode (13.3 MB/s max.) 8-bit mode (26.6 MB/s max.) 16-bit mode REQ Period ≥ 75 ns ACK Period ≥ 75 ns
		X'13' (76 ns) : X'19'(100 ns)	SDTR Transfer Period = Specified value by INIT	Synchronous mode (10.0 MB/s max.) 8-bit mode (20.0 MB/s max.) 16-bit mode REQ Period ≥ 100 ns ACK Period ≥100 ns
		X'1A' (104 ns) : X'1F' (124 ns)	SDTR Transfer Period =Specified value by INIT	Synchronous mode (8.00 MB/s max.) 8-bit mode (16.0 MB/s max.) 16-bit mode REQ Period ≥ 125 ns ACK Period ≥ Specified value by INIT
		X'20' (128 ns) : X'25' (148 ns)	SDTR Transfer Period =Specified value by INIT	Synchronous mode (6.67 MB/s max.) 8-bit mode (13.33 MB/s max.) 16-bit mode REQ Period ≥ 150 ns ACK Period ≥ Specified value by INIT
		X'26' (152 ns) : X'2B' (172 ns)	SDTR Transfer Period =Specified value by INIT	Synchronous mode (5.71 MB/s max.) 8-bit mode (11.42 MB/s max.) 16-bit mode REQ Period ≥ 175 ns ACK Period ≥ Specified value by INIT
		X'2C' (176 ns) : X'32' (200 ns)	SDTR Transfer Period =Specified value by INIT	Synchronous mode (5.00 MB/s max.) 8-bit mode (10.00 MB/s max.) 16-bit mode REQ Period ≥ 200 ns ACK Period ≥ Specified value by INIT
		X'33' (204 ns) : X'FF' (1020 ns)	Respond with offset=0	Asynchronous mode

d. Transfer mode setup from IDD to INIT

When the synchronous data transfer mode is allowed by the CHANGE CONDITION command, the IDD shall execute one of the following operations if the INIT still continue the default transfer mode.

(a) When the ATTENTION condition has been generated:

If an ATTENTION condition exists before the COMMAND phase and if the INIT does not send the SYNCHRONOUS DATA TRANSFER REQUEST message after the end of COMMAND phase, the IDD shall try to select the synchronous data transfer mode by sending the SYNCHRONOUS DATA TRANSFER REQUEST message to the INIT.

Table 2.6 shows the contents of the SYNCHRONOUS DATA TRANSFER REQUEST message sent from the IDD and the data transfer mode set to the IDD and INIT by the response of this message from the INIT. If the INIT does not respond as defined on Table 2.6, the IDD assumes that the synchronous data transfer is unavailable and selects the asynchronous data transfer mode between the IDD and the INIT.

If an ATTENTION condition has occurred in the COMMAND phase and if the IDD has entered the BUS FREE phase or STATUS phase as the result of MESSAGE OUT phase operations, the default transfer mode of the INIT continues when the IDD cannot send the SYNCHRONOUS DATA TRANSFER REQUEST message.

(b) When the ATTENTION condition has not been generated:

If the ATTENTION condition does not exist, the IDD does not send the SYNCHRONOUS DATA TRANSFER REQUEST message to the INIT. In this case, data is transferred in the asynchronous transfer mode. The default transfer mode of the INIT is released.

Table 2.6 Transfer mode setup request from IDD to INIT

(SDTR: SYNCHRONOUS DATA TRANSFER REQUEST message)

Message from IDD		Response from INIT			Transfer mode to be defined
SDTR REQ/ACK Offset = X'7F'		MESSAGE REJECT			Asynchronous mode
		S D T R	REQ/ACK Offset	X'00'	Asynchronous mode
				X'01' : X'7F'	Synchronous mode REQ/ACK offset ≤ Specified value by INIT
				X'80' :	REQ/ACK offset= X'7F'
Transfer Period = X'0A' (25 ns) (LVD mode)			Transfer Period	X'00' : X'09'	Synchronous mode (40.0 MB/s max.) 8-bit mode (80.0 MB/s max.) 16-bit mode REQ Period ≥ 25 ns ACK Period ≥ 25 ns
				X'0A' (25 ns)	Synchronous mode (40.0 MB/s max.) 8-bit mode (80.0 MB/s max.) 16-bit mode REQ Period ≥ 25 ns ACK Period ≥ Specified value by Init
				X'0B' (50.0 ns)	Synchronous mode (20.0 MB/s max.) 8-bit mode (40.0 MB/s max.) 16-bit mode REQ Period ≥ 50.0 ns ACK Period ≥ Specified value by Init
	Transfer Period = X'0C' (50 ns) (SE mode)			X'0C' (50 ns)	Synchronous mode (20.0 MB/s max.) 8-bit mode (40.0 MB/s max.) 16-bit mode REQ Period ≥ 50 ns ACK Period ≥ Specified value by INIT
				X'0D' : X'12' (72 ns)	Synchronous mode (13.3 MB/s max.) 8-bit mode (26.6 MB/s max.) 16-bit mode REQ Period ≥ 75 ns ACK Period ≥ Specified value by INIT
				X'13' (76 ns) : X'19'(100 ns)	Synchronous mode (10.0 MB/s max.) 8-bit mode (20.0 MB/s max.) 16-bit mode REQ Period ≥ 100 ns ACK Period ≥ Specified value by INIT
				X'1A' (104 ns) : X'1F' (124 ns)	Synchronous mode (8.00 MB/s max.) 8-bit mode (16.0 MB/s max.) 16-bit mode REQ Period ≥ 125 ns ACK Period ≥ Specified value by INIT
				X'20' (128 ns) : X'25' (148 ns)	Synchronous mode (6.67 MB/s max.) 8-bit mode (13.33 MB/s max.) 16-bit mode REQ Period ≥ 150 ns ACK Period ≥ Specified value by INIT
				X'26' (152 ns) : X'2B' (172 ns)	Synchronous mode (5.71 MB/s max.) 8-bit mode (11.42 MB/s max.) 16-bit mode REQ Period ≥ 175 ns ACK Period ≥ Specified value by INIT
				X'2C' (176 ns) : X'32' (200 ns)	Synchronous mode (5.00 MB/s max.) 8-bit mode (10.00 MB/s max.) 16-bit mode REQ Period ≥ 200 ns ACK Period ≥ Specified value by INIT
				X'33' (204 ns) : X'FF' (1020 ns)	Asynchronous mode (*1)

*1 If the INIT responds to these values during transfer period with non-zero and REQ/ACK offset, the IDD sends the MESSAGE REJECT message following the INIT's SYNCHRONOUS TRANSFER REQUEST message and forcibly switches the synchronous transfer mode to the asynchronous transfer mode.

2.3.21 WIDE DATA TRANSFER REQUEST message (I↔T)

Byte	0	1	2	3
	X'01'	X'02'	X'03'	m

m: Transfer Width Exponent
Transfer width = 2^m bytes

Two SCSI devices exchange the WIDE DATA TRANSFER REQUEST message to determine the data bus width between them.

When an SCSI device that supports the wide mode data transfer connects to other SCSI device just after power-on, after the RESET condition occurs, or after it receives the TARGET RESET message, it exchanges this message to determine the wide mode data transfer. Each SCSI device shall always respond to this message exchange request any time when it is issued from another SCSI device.

The data bus width between two SCSI devices is determined by the exchange of WIDE DATA TRANSFER REQUEST message. The determined data bus width is applied to the DATA IN and DATA OUT phases only. In another INFORMATION TRANSFER phase, data is transferred over the 8-bit bus data.

If an SCSI device supports both the synchronous data transfer and the wide mode transfer, it shall exchange the WIDE DATA TRANSFER REQUEST message with another SCSI device before exchanging the SYNCHRONOUS DATA TRANSFER REQUEST message.

If the SCSI device having the wide mode transfer function receives the WIDE DATA TRANSFER REQUEST message, the data transfer mode is reset to the asynchronous transfer mode.

(1) Wide mode parameters

The data bus width between two SCSI devices is determined by exchanging the WIDE DATA TRANSFER REQUEST message. This value applies to all logical units assigned to these two SCSI devices.

The valid data bus width is determined by the Transfer Width Exponent value.

An SCSI device, which sends this message first, specifies the maximum possible data bus width and sends the WIDE DATA TRANSFER REQUEST message. The destination SCSI device returns the same value if it can support the requested data bus width. If impossible, the destination SCSI device answers the possible data bus width.

After the WIDE DATA TRANSFER REQUEST messages have been exchanged normally, the two SCSI devices shall set the data bus width based on the response (the return message) by the SCSI device which has first received the message. Table 2.7 defines the data bus width to be set by message exchange.

Table 2.7 Data bus width defined by message exchange

Response message	Data bus width
WIDE DATA TRANSFER REQUEST Transfer Width Exponent > 1	Data is transferred using the responded data bus width.
WIDE DATA TRANSFER REQUEST Transfer Width Exponent = 0	8-bit data transfer
MESSAGE REJECT message	8-bit data transfer

(2) Message exchange started by the INIT

If the INIT needs to select the wide data transfer mode, it asserts the ATN signal to start message exchange. Then, the INIT requests the TARG to receive the WIDE DATA TRANSFER REQUEST message. When the MESSAGE OUT phase has terminated normally, the TARG shall return an appropriate WIDE DATA TRANSFER REQUEST message to the INIT. If the TARG cannot return the message normally, these two SCSI devices shall set the 8-bit data bus width between them.

If the INIT asserts the ATN signal in the MESSAGE IN phase and sends the MESSAGE REJECT message even if the TARG returns a WIDE DATA TRANSFER REQUEST message which indicates a non-zero value in its Transfer Width Exponent field, the two SCSI devices shall set the 8-bit data bus width between them.

If the INIT sends the MESSAGE PARITY ERROR message or the INITIATOR DETECTED ERROR message against the TARG'S WIDE DATA TRANSFER REQUEST message, the IDD recognizes that there was a parity error in the previous MESSAGE IN phase. Then the IDD performs the error recovery procedure based on the SCSI Bus protocol for the erroneous phase up to 3 times. If the retry fails, this negotiation is regarded as a failure. The mode setting for wide transfer between the INIT and the TARG must be set to the 8-bit data bus width.

(3) Message exchange started by the TARG

If the TARG recognizes the need of message exchange and if the wide data mode transfer request is enabled by the CHANGE DEFINITION command, the TARG sends the WIDE DATA TRANSFER REQUEST message to the INIT. The INIT shall assert the ATN signal and return the WIDE DATA TRANSFER REQUEST message or the MESSAGE REJECT message before negating the ACK signal of the last byte of WIDE DATA TRANSFER REQUEST message which has been sent from the TARG. If the INIT cannot respond to this message, the two SCSI devices shall set the 8-bit data bus width between them.

Both the INIT and the TARG shall not consider the completion of WIDE DATA TRANSFER REQUEST message exchange until the TARG terminates the MESSAGE OUT phase by entering another INFORMATION TRANSFER phase (which indicates that no parity error has been detected) even if the INIT responds with the WIDE DATA TRANSFER REQUEST message. If the TARG cannot normally receive a response message by the INIT after the specified number of retries, the TARG shall immediately negate the BSY signal and enter the BUS FREE phase without starting another INFORMATION TRANSFER phase.

The INIT shall consider it as the unsuccessful message exchange, and the two SCSI devices shall set the 8-bit data bus width between them.

If the TARG enters the MESSAGE IN phase and first sends the MESSAGE REJECT message to the INIT immediately after the INIT has responded with the WIDE DATA TRANSFER REQUEST message, such message exchange is made invalid and the two SCSI devices shall set the 8-bit data bus width between them.

(4) Valid period of wide data transfer mode

After the exchange of WIDE DATA TRANSFER REQUEST message, the data bus width determined between the two SCSI devices shall be kept valid until when:

- TARGET RESET MESSAGE reception
- RESET condition ("hardware RESET") occurrence
- Transfer width change between the same SCSI devices
- Power turned off
- Change in the transceiver mode (e.g., LVD mode to SE mode).

The default data bus width is 8 bits between SCSI devices. The data bus width shall be initialized to 8 bits when the power supply is turned on, a TARGET RESET message is received, or when a RESET condition occurs.

(5) Wide mode transfer of IDD

a. Mode setting

When the IDD recognizes the wide mode data transfer to be set, the INIT can select whether the IDD sends the WIDE DATA TRANSFER REQUEST message to the INIT by sending the CHANGE DEFINITION command.

For details on setting, refer to Section 3.1.4 in the SCSI Logical Specifications.

b. Data bus width status determination

(a) Default 8-bit mode status

The default 8-bit data bus width mode is selected automatically when the power supply is turned on, a RESET condition occurs, or the TARGET RESET message is received (initial state). Each INIT has this default bus width mode. When the WIDE DATA TRANSFER REQUEST message is first exchanged between SCSI devices, the 8-bit or 16-bit data bus width is set between them.

(b) Data bus width determination status

This status occurs when the default data transfer mode has been released and a data bus width has been determined. This status can be set on each INIT, and the data bus width of each INIT may differ.

Data is transferred within the data bus width set to the INIT based on the SCSI ID of the INIT which is identified in the SELECTION phase.

If the INIT is in this state, the IDD does not request for a change of data bus width. If its change is requested by the INIT, the IDD shall respond to it and change the data bus width. When changing the WIDE DATA TRANSFER REQUEST message, if the setting sequence

ended in error, the transfer width between it and the INIT, and the synchronous mode will change to the default transfer mode.

Note:

When the INIT requests for a change of data bus width, the IDD responds to the request. At this time, the current synchronous transfer mode is reset to the default asynchronous transfer mode. If the INIT wishes to start data transfer in the synchronous transfer mode, the INIT and the IDD shall exchange the SYNCHRONOUS DATA TRANSFER REQUEST message after the exchange of WIDE DATA TRANSFER REQUEST message.

c. Wide mode setting from the INIT to the IDD

Table 2.8 lists the responses by the IDD when the INIT first sends the WIDE DATA TRANSFER REQUEST message for request of data bus width setup. Also, this table lists the data bus width to be set between the INIT and IDD, depending on the IDD response to the message.

Table 2.8 Wide mode setting request from the INIT to the IDD

Message from INIT		Response message from IDD	Transfer width to be set
WDTR	X'00'	Transfer Width Exponent = '00'	8-bit width
	X'01'	Transfer Width Exponent = '00'	8-bit width
		Transfer Width Exponent = '01'	16-bit width
	X'02' or larger	Transfer Width Exponent = '01'	16-bit width

d. Wide mode setting from the IDD to the INIT

If the WIDE DATA TRANSFER REQUEST message is enabled to send by the CHANGE DEFINITION command, and if the default 8-bit data bus width mode has been selected between the IDD and the INIT, the IDD executes one of the following operations when it receives the command from the INIT:

(a) With ATTENTION condition

If the IDD cannot receive the WIDE DATA TRANSFER REQUEST message form the INIT after the COMMAND phase has completed, the IDD tries to set the data bus width by sending the WIDE DATA TRANSFER REQUEST message to the INIT.

Table 2.9 lists the contents of WIDE DATA TRANSFER REQUEST message to be sent by the IDD, and the data bus width to be set between the IDD and INIT when the message is responded by the INIT.

If the INIT does not respond to the WIDE DATA TRANSFER REQUEST message, the IDD considers that the wide mode data transfer is impossible and sets the 8-bit data bus width between the IDD and the INIT.

However, on the LVD machine in the 8-bit fixed mode (13 and 14 of CN2 are shorted), the IDD does not send the WIDE DATA TRANSFER REQUEST message.

(b) Without ATTENTION condition

If the ATTENTION condition does not exist, the IDD does not send the WIDE DATA TRANSFER REQUEST message to the INIT. In such case, the 8-bit bus width is set between the IDD and the INIT.

Table 2.9 Wide mode setting request from the IDD to the INIT

Message from TARG		Response message from IDD	Transfer width to be set
WDTR	Transfer Width	MESSAGE REJECT	8-bit width
		X'00'	8-bit width
	Exponent = X'01'	X'01'	16-bit width
		X'02' or larger	16-bit width

2.3.22 PARALLEL PROTOCOL REQUEST message (I↔T)

Byte	0	1	2	3	4	5	6	7
	X'01'	X'06'	X'04'	m	X'00'	n	x	y

m: Transfer Period Factor [4 × m (ns)]
n: REQ/ACK OFFSET
x: Transfer Width Exponent
Transfer width = 2^x bytes
y: Protocol Options Bit

Bit	7	6	5	4	3	2	1	0
Byte7	PCMP_EN	RTI	RD_STRM	WR_FLOW	HOLD_MCS	QAS_REQ	DT_REQ	IU_REQ

PCMP_EN : Precompensation Enable
RTI : Retain Training Information
RD_STRM : Read Streaming
WR_FLOW : Write Flow Control
HOLD_MCS : Hold Margin Control Settings
QAS_REQ : Quick Arbitration Request
DT_REQ : Double Transfer Request
IU_REQ : Information Unit Request

The PARALLEL PROTOCOL REQUEST messages are used to negotiate a synchronous data transfer agreement, a wide data transfer agreement, and set the protocol options between two SCSI devices.

Note:

ST synchronous data transfer (Single Transfer)
DT synchronous data transfer (Double Transfer)

Table 2.10 TRANSFER PERIOD FACTOR field

CODE	DESCRIPTION
X'00'-X'07'	Reserved
X'08'	Transfer period equals 6.25ns (note 2). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports precompensation, information units, and double-transition data transfers.
X'09'	Transfer period equals 12.5ns (note 3). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
X'0A'	Transfer period equals 25ns (note 4)
X'0B'	Transfer period equals 50.0ns (note 4)
X'0C'	Transfer period equals 50ns (note 5)
X'00'-X'18'	Transfer period equals the period factor (note 5)
X'19'-X'31'	Transfer period equals the period factor (note 6)
X'32'-X'FF'	Transfer period equals the period factor (note 6)

Notes:

1. Fast-160 data is latch every 6.25ns.
2. Fast-80 data is latched every 12.5 ns.
3. Fast-40 data is latched every 25 ns or 50.0 ns.
4. Fast-20 data is latched using a transfer period of less than or equal 96 ns and greater than or equal to 50 ns.
5. Fast-10 data is latched using a transfer period of less than or equal 196 ns and greater than or equal 100 ns.
6. Fast-5 data is latched using a transfer period of less than or equal 1,020 ns and greater than or equal to 200 ns.

For ST synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ assertions allowed to be outstanding before a corresponding ACK assertion is received at the TARG. The size of a data transfer may be 1or 2 bytes depending on the values in the transfer width exponent field.

For DT synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ transitions allowed to be outstanding before a corresponding ACK transition is received at the TARG. The size of a data transfer shall be 2 bytes.

See Section 1.5 for an explanation of the differences between DT and ST data transfers.

The REQ/ACK OFFSET value is chosen to prevent overflow conditions in the SCSI device's reception buffer and offset counter. A REQ/ACK OFFSET value of zero shall indicate asynchronous data transfer mode and that the PERIOD FACTOR field and the PROTOCOL OPTIONS field shall be ignored; a value of FFh shall indicate unlimited REQ/ACK offset.

The TRANSFER WIDTH EXPONENT field defines the transfer width to be used during DATA IN phases, and DATA OUT phases. The transfer width that is established applies to all logical units on both SCSI devices.

Valid transfer widths are 8 bits (m=00h) and 16 bits (m=01h) if all the protocol options bits are zero. The only valid transfer width is 16 bits (m=01h) if any of the protocol options bits are one. TRANSFER WIDTH EXPONENT field values greater than 01h are reserved.

The protocol options bits (PCOMP_EN, RTI, RD_STRM, WR_FLOW, IU_REQ, DT_REQ, QAS_REQ, and HOLD_MCS) are used by the originating SCSI device to indicate the protocol options to be enabled. The responding SCSI device uses the protocol options bits to indicate the protocol options requested by the originating SCSI device the responding SCSI device has enabled.

INIT shall set PCOMP_EN to one to indicate that the TARG shall enable precompensation on all signals transmitted during DT DATA phases. The INIT shall set PCOMP_EN to zero to indicate that the SCSI target port shall disable precompensation.

TARG shall set PCOMP_EN to one to indicate that the INIT shall enable precompensation on all signals transmitted during DT DATA phases. The TARG shall set PCOMP_EN to zero to indicate that the INIT shall disable precompensation.

Ports that support Fast-160 shall support enabling and disabling precompensation of their drivers. For negotiated transfer periods slower than Fast-160 the PCOMP_EN bit shall be set to zero.

Note :

Unlike other fields and bits in the PPR message the PCOMP_EN bit is not a negotiated value; instead, it instructs the receiving SCSI device as to whether or not precompensation is to be disabled or enabled. Because of this, precompensation may be enabled on one of the SCSI devices and disabled on the other SCSI device at the completion of a successful PPR negotiation.

INIT shall set RD_STRM to one to indicate that the TARG should enable read streaming and read flow control. In response, the TARG shall set RD_STRM to one if it is capable of read streaming and read flow control and zero if it is not.

The INIT shall set RD_STRM to zero to indicate that the TARG shall disable read streaming and read flow control. In response, the TARG shall set RD_STRM to zero.

Read streaming and read flow control only occur during information unit transfers.

INIT shall set WR_FLOW to one to indicate that the TARG should enable write flow control during write streaming. In response, the TARG shall set WR_FLOW to one if it is capable of write flow control and zero if it is not.

The INIT shall set WR_FLOW to zero to indicate that the TARG shall disable write flow control during write streaming. In response, the TARG shall set WR_FLOW to zero.

Write streaming and write flow control only occurs during information unit transfers.

An information units enable request bit (IU_REQ) of zero indicates that information unit transfers shall not be used (i.e., data group transfers shall be enabled) when received from the originating SCSI device and that information unit transfers are not supported when received from the responding SCSI device. An IU_REQ bit of one indicates that information unit transfers shall be used when received from the originating SCSI device and that information unit transfers are supported when received from the responding SCSI device. If the IU_REQ bit is changed from the previous agreement (i.e., zero to one or one to zero) as a result of a negotiation the TARG shall go to a BUS FREE phase on completion of the negotiation.

A DT enable request bit (DT_REQ) of zero indicates that DT DATA phases are to be disabled when received from the originating SCSI device and that DT DATA phases are not supported when received from the responding SCSI device. An DT_REQ bit of one indicates that DT DATA phases are to be enabled when received from the originating SCSI device and that DT DATA phases are supported when received from the responding SCSI device.

A QAS enable request bit (QAS_REQ) of zero indicates that QAS is to be disabled when received from the originating SCSI device and that QAS is not supported when received from the responding SCSI device.

The INIT shall set HOLD_MCS to one to indicate that the TARG should hold any margin control settings set with the MARGIN CONTROL SUBPAGE of the PORT CONTROL MODE PAGE (see LOGICAL SPECIFICATION). In response, the TARG shall set HOLD_MCS to one if it is capable of retaining the settings and zero if it is not.

When the INIT shall set HOLD_MCS to zero to indicate that the TARG should reset this mode page.

Not all combinations of the protocol options bits are valid. Only the bit combinations defined in table 2.11 shall be allowed all allowed. All other combinations are reserved.

Table 2.11 Valid protocol options bit combinations

PCMP_EN	RTI	RD_STRM	WR_FLOW	HOLD_MCS	QAS_REQ	DT_REQ	IU_REQ	DESCRIPTION
0	0	0	0	0/1	0	0	0	Use ST DATA IN and ST DATA OUT phases to transfer data
0	0	0	0	0/1	1	0	0	Use DT DATA IN and DT DATA OUT phases with data group transfers
0	0	0	0	0/1	1	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers and QAS arbitration.
1	0/1	0/1	0/1	0/1	1	0	1	Use DT DATA IN and DT DATA OUT phases with information unit transfer.
1	0/1	0/1	0/1	0/1	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfer. And QAS arbitration.

A PARALLEL PROTOCOL REQUEST agreement applies to all logical units of the two SCSI devices that negotiated agreement. That is, if SCSI device A, acting as an INIT negotiates a data transfer agreement with SCSI device B (a TARG), then the same data transfer agreement applies to SCSI devices A and B even if SCSI device B changes to an INIT.

A data transfer agreement only applies to the two SCSI devices that negotiate the agreement. Separate data transfer agreements are negotiated for each pair of SCSI devices. The data transfer agreement only applies to DATA phases and information unit transfers.

A PARALLEL PROTOCOL REQUEST message exchange shall be initiated by a SCSI device whenever a previously arranged parallel protocol agreement may have become invalid. The agreement becomes invalid after any condition that may leave the parallel protocol agreement in an indeterminate state such as:

a) RESET condition ("hardware RESET") occurrence
b) TARGET RESET message reception
c) Power turned off
d) Change in the transceiver mode (e.g., LVD mode to SE mode)

Any condition that leaves the data transfer agreement in an indeterminate state shall cause the SCSI device to enter an asynchronous, eight-bit wide data transfer mode with all the protocol options bits set to set to zero.

A SCSI device may initiate a PARALLEL PROTOCOL REQUEST message exchange whenever it is appropriate to negotiate a data transfer agreement. SCSI devices that are currently capable of supporting any of the PARALLEL PROTOCOL REQUEST options shall not respond to a PARALLEL PROTOCOL REQUEST message with a MESSAGE REJECT message.

Renegotiation after every selection is not recommended, since a significant performance impact is likely. The PARALLEL PROTOCOL REQUEST message exchange establishes an agreement between the two SCSI devices;

a) on the permissible periods and the REQ/ACK offsets for all logical units on the two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other phases shall use asynchronous transfers;

b) on the width of the data path to be used for DATA phase transfers between two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other information transfer phases shall use an eight-bit data path; and

c) on the protocol option is to be used. The originating SCSI device (the SCSI device that sends the first of the pair of PARALLEL PROTOCOL REQUEST messages) sets its values according to the rules above to permit it to receive data successfully.

If the responding SCSI device is able to receive data successfully with these values (or smaller periods or larger REQ/ACK offsets or both), it returns the same values in its PARALLEL PROTOCOL REQUEST message. If it requires a larger period, a smaller REQ/ACK offset, or a smaller transfer width in order to receive data successfully, it substitutes values in its PARALLEL PROTOCOL REQUEST message as required, returning unchanged any value not required to be changed. Each SCSI device when transmitting data shall respect the negotiated limits set by the other's PARALLEL PROTOCOL REQUEST message, but it is permitted to transfer data with larger periods, smaller synchronous REQ/ACK offsets, or both. The completion of an exchange of PARALLEL PROTOCOL REQUEST messages implies an agreement as shown in Table 2.12

If the responding SCSI device does not support the selected protocol option it shall clear as many bits as required to set the protocol option field to a legal value that it does support.

If there is an unrecoverable parity error on the initial PARALLEL PROTOCOL REQUEST message the initiating SCSI device shall retain its previous data transfer mode and protocol options. If there is an unexpected bus free on the initial PARALLEL PROTOCOL REQUEST message the initiating SCSI device shall retain its previous data transfer mode and protocol options.

Table 2.12 PARALLEL PROTOCOL REQUEST message implied agreement

Responding SCSI device PARALLEL PROTOCOL REQUEST response	Implied agreement
Non-zero REQ/ACK offset	Synchronous transfer (i.e., Each SCSI device transmits data with a period equal to or greater than and a REQ/ACK offset equal to or less than the negotiated values received in the responding SCSI device's PPR message).
REQ/ACK offset equal to zero	Asynchronous transfer
Non-zero TRANSFER WIDTH EXPONENT	Wide transfer (i.e., the initiator and the target transmit data with a transfer width equal to the responding device's transfer width). If the initiating SCSI device does not support the responding SCSI device's TRANSFER WIDTH EXPONENT then the initiating SCSI device shall MESSAGE REJECT the PPR message.
TRANSFER WIDTH equal to zero	Eight-bit data
Protocol options equal to 0h and transfer period factor equal to 9h	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
IU_REQ, DT_REQ, and QAS_REQ Equal to zero	ST DATA IN and ST DATA OUT phases to transfer data
DT_REQ equal to one	DT DATA IN and DT DATA OUT phases transfer data with IU RC
IU_REQ, and DT_REQ equal to one	DT DATA IN and DT DATA OUT phases with information units
MESSAGE REJECT message	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
Parity error (on responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
Unexpected bus free (as a result of the responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
No response	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h

(1) Target initiated PARALLEL PROTOCOL REQUEST negotiation

If the TARG recognizes that PARALLEL PROTOCOL REQUEST negotiation is required, it not sends a PARALLEL PROTOCOL REQUEST message to the INIT.

(2) Initiator initiated PARALLEL PROTOCOL REQUEST negotiation

If the INIT recognizes that PARALLEL PROTOCOL REQUEST negotiation is required, it creates an attention condition and sends a PARALLEL PROTOCOL REQUEST message to begin the negotiating process. After successfully completing the MESSAGE OUT phase, the TARG shall respond with a PARALLEL PROTOCOL REQUEST message or a MESSAGE REJECT message.

If an abnormal condition prevents the TARG from responding with a PARALLEL PROTOCOL REQUEST message or with a MESSGE REJECT message then both SCSI devices shall use the eight-bit/asynchronous data transfer mode with all the protocol options bits set zero to indicate ST DATA IN and ST DATA OUT phases between the two SCSI devices.

Following a TARG's responding PARALLEL PROTOCOL REQUEST message, an implied agreement for data transfers shall not be considered to exist until;

a) the INIT receives the last byte of the PARALLEL PROTOCOL REQUEST message and parity is valid; and

b) the TARG does not detect an attention condition on the last byte of the PARALLEL PROTOCOL REQUEST message.

If the INIT does not support the TARG’s responding PARALLEL PROTOCOL REQUEST message’s values the INIT shall create an attention condition and the first message shall be a MESSAGE REJECT message.

If during the PARALLEL PROTOCOL REQUEST message the INIT creates an attention condition and the first message of the MESSAGE OUT phase is either a MESSAGE PARITY ERROR or MESSAGE REJECT message the data transfers shall be considered to be negated by both SCSI devices. In this case, both SCSI devices shall use the go to eight-bit/asynchronous data transfer mode with all the protocol options bits set zero to indicate ST DATA IN and ST DATA OUT phases for data transfers between the two SCSI devices.

CHAPTER 3 ERROR RECOVERY

This chapter describes the SCSI bus errors and their recovery by the IDD.

Note:

If a severe error has occurred, the IDD may switch the SCSI bus to the BUS FREE phase without sending the DISCONNECT or TASK COMPLETE message to the INIT. In such case, the IDD clears all information of the currently executing commands and does not report the command completion (or reconnection) to the INIT.

If the SCSI bus is switched to the BUS FREE phase in a sequence other than the normal bus sequence, the INIT shall consider that the currently executing command has terminated abnormally. In such case, the IDD may or may not generate a sense data of this error. However, the INIT should issue the REQUEST SENSE command to obtain the error information.

3.1 Error Conditions and Retry Procedure

(1) MESSAGE OUT phase parity error

When the IDD detects a parity error of the SCSI bus during the MESSAGE OUT phase, it retries the MESSAGE OUT phase up to 3 times. If the IDD fails to recover a parity error, it proceeds to the next procedure. For details, see Section 1.6.9.

If the LUN is already identified, the IDD terminates the currently executing command with the CHECK CONDITION status. At this time, the sense key/sense code of the sense data indicates the "ABORTED COMMAND [=B]/SCSI parity error [=47-00]." If this happens after the status is reported, the IDD enters the BUS FREE phase and the same sense data is retained. The IDD ignores the ATTENTION condition until it enters the BUS FREE phase. If the LUN is not identified by the IDENTIFY message or the LUN field of CDB, the IDD does not generate the sense data and enters the BUS FREE phase immediately.

(2) COMMAND phase parity error

When the IDD detects a parity error in the COMMAND phase, it retries the Command Phase up to 3 times. If the IDD fails to recover a parity error, it proceeds to the next procedure.

If the LUN is already identified by the IDENTIFY message, the IDD terminates the command with the CHECK CONDITION status. The sense key/sense code of the sense data indicates the "ABORTED COMMAND [=B]/SCSI parity error [=47-00]."

If the LUN is not identified, the IDD does not generate the sense data and enters the BUS FREE phase immediately.

(3) DATA OUT phase parity error

When the IDD detects a parity error of SCSI bus in the DATA OUT phase, it does not make retry and proceeds to the next procedure.

The IDD terminates the currently executing command with the CHECK CONDITION status. The sense key/sense code of the sense data indicates the "ABORTED COMMAND [=B]/SCSI parity error [=47-00]."

(4) Receiving a INITIATOR DETECTED ERROR message

When the IDD receives an INITIATOR DETECTED ERROR message from the INIT, except for the Data Phase and the Message Out Phase, it retries the previous phase up to 3 times. If the recovery sequence is failed or not done, the IDD proceeds to the next procedure.

If the LUN is already identified, the IDD terminates the currently executing command with the CHECK CONDITION status. The sense key/sense code of the sense data indicates the "ABORTED COMMAND [=B]/INITIATOR DETECTED ERROR message received [=48-00]." If the LUN is not identified yet, the IDD does not generate the sense data and enters the BUS FREE phase immediately. If the STATUS phase has already completed, the IDD also enters the BUS FREE phase but does not send the status again.

(5) Receiving a MESSAGE PARITY ERROR message

If the IDD receives a MESSAGE PARITY ERROR message from the INIT as its response to the ATTENTION condition (MESSAGE OUT phase) generated at the MESSAGE IN phase execution, the IDD recognizes that there was a parity error in the previous MESSAGE IN phase. Then the IDD performs the error recovery procedure based on the SCSI Bus protocol for the previous MESSAGE IN phase up to 3 times. If the retry fails, the IDD enters the BUS FREE phase immediately and terminates the executing command abnormally. The IDD does not report the command completion (that is, the IDD does not send the status and TASK COMPLETE message) of that command. If the LUN is identified before the error occurrence, the IDD generates the sense data which indicates the "ABORTED COMMAND [=B]/SCSI parity error [=47-00]" sense key/sense code. If the LUN is not identified, no sense data is generated.

If the IDD receives a MESSAGE PARITY ERROR message from the INIT as its response to that ATTENTION condition generated at execution of other than the MESSAGE IN phase, the IDD enters the STATUS phase immediately. If the LUN is identified before the error occurrence, the IDD generates the sense data which indicates the "ABORTED COMMAND [=B]/Invalid message error [=49-00]" sense key/sense code.

(6) Rejected messages

When the IDD receives a MESSAGE REJECT message from the INIT, the IDD executes one of the following depending on the rejected message type:

a. TASK COMPLETE

The IDD enters the BUS FREE phase immediately, and does not consider this as an error.

b. DISCONNECT

The IDD does not perform the disconnection of the SCSI bus at this time and continues the currently executing command with keeping connection with the SCSI bus. However, the IDD may send the DISCONNECT message to attempt to disconnect during the command execution if the INIT indicates in the IDENTIFY message that it supports the disconnect/ reconnect function.

c. IDENTIFY

When this message sent for reconnection is rejected, the IDD immediately enters the BUS FREE phase and terminates the command which has requested the reconnection abnormally. No further reconnection for the command is attempted, and the IDD does not report the command completion (status and message). At this time, the IDD creates the sense information with Sense Key/Additional Sense Code of "ABORTED COMMAND [=B]/Message Error [=43-00]".

d. LINKED TASK COMPLETE

The IDD immediately enters the BUS FREE phase without requesting the next linked command (CDB). The command link is broken. Then, the IDD creates the sense information for the INIT with Sense Key/Additional Sense Code of "ABORTED COMMAND [=B]/Message Error [=43-00]".

e. MESSAGE REJECT

When the LUN is already identified, the IDD immediately terminates the currently executing command with CHECK CONDITION status and with the Sense Key/Additional Sense Code of "ABORTED COMMAND [=B]/Message Error [=43-00]".

When the LUN has not been identified, the IDD immediately enters the BUS FREE phase without generating sense data.

f. RESTORE POINTERS

The IDD sends this message during the error recovery procedure for the COMMAND phase or the STATUS phase. If the RESTORE POINTERS message is rejected, the IDD regards the result of the recovery procedure as a failure.

g. SAVE DATA POINTER

When rejecting this message for disconnection of the SCSI bus, the IDD continues the currently executing command without disconnection as the DISCONNECT message is rejected.

h. SIMPLE

When this message sent next to the IDENTIFY message at reconnection is rejected, the IDD immediately enters the BUS FREE phase and terminates the command which has requested the reconnection abnormally. No further reconnection for the command is attempted, and the IDD does report the command completion (status and message) for the aborted command. Then, the IDD creates the sense information with Sense Key/Additional Sense Code of "ABORTED COMMAND [=B]/Message Error [=43-00]".

i. SYNCHRONOUS DATA TRANSFER REQUEST

The IDD assumes that the INIT does not support the synchronous transfer mode, and continues the command execution using the asynchronous transfer mode.

j. WIDE DATA TRANSFER REQUEST

The IDD assumes that the INIT does not support the wide transfer mode. The IDD sets the data transfer width to the 8-bit mode and the asynchronous mode, and continues command execution.

k. PARALLEL PROTOCOL REQUEST

The IDD assumes that the INIT does not support the DT DATA IN/OUT transfer mode. The IDD sets the data transfer mode to the 8-bit width mode and the asynchronous mode, and continues command execution.

(7) Reselection timeout

If the INIT does not respond within the specified time period (Selection Timeout Delay: 250 ms) in the RESELECTION phase, the IDD considers that a reselection timeout has occurred. In this case, the IDD executes timeout processing of RESELECTION phase based on the protocol of SCSI bus phase, and it enters the BUS FREE phase. (For the timeout processing, see Section 1.6.4.)

After entering the BUS FREE phase, the IDD waits at least 200 μs and retries the reselection.

If the reselection retries have failed, the IDD abnormally terminates the command which is requiring the reconnection. In such case, the command is never reconnected and the IDD does not report the command completion (the status and message). The IDD generates the sense data which indicates the "ABORTED COMMAND [=B]/Select/reselect failure [=45-00]" sense key/sense code.

Note:

The retry count for the timeout of RESELECTION phase can be set by the CHANGE DEFINITION command. For details, see Section 1.6.11.

(8) Errors concerning message protocol

If the IDD detects an ATTENTION condition in the SELECTION phase and it receives the message except for the following messages from the INIT in its response to the ATTENTION condition (the MESSAGE OUT phase), the IDD considers it as an error in the message protocol and enters the BUS FREE phase immediately.

- IDENTIFY
- ABORT TASK
- TARGET REST

(9) Internal controller error

If a hardware or firmware error inside of the IDD is detected and if the LUN is already identified, the IDD abnormally terminates the currently executing command in the CHECK CONDITION status. In such case, the IDD generates the sense data which indicates the "HARDWARE ERROR [=4]/Internal target failure [=44-nn]" sense key/sense code. If the LUN is not identified yet, the IDD does not generate the sense data but enters the BUS FREE phase immediately.

3.2 Recovery Control

The IDD performs the error recovery for some kinds of SCSI bus errors (see Section 3.1). All recovery procedures are based on the protocol of SCSI bus phase.

Note:

If the INIT does not generate an ATTENTION condition, the IDD does not use any message except for the TASK COMPLETE message. Also, the IDD does not execute the MESSAGE OUT phase. If a parity error is detected in the COMMAND phase, the IDD considers that the LUN is not identified and it enters the BUS FREE phase immediately.

Table 3.1 gives and outline of the retry procedure for handling SCSI bus errors. If the IDD performs the error recovery, Table 3.1 means the operation after the error recovery fails. The symbols used in this table are as follows.

LUN	I	:	An LUN is already identified.
	N	:	An LUN is not yet.
	X	:	Don’t care
GOOD		:	GOOD status
CHECK		:	CHECK CONDITION status If the STATUS phase is already executed in the current I/O process, the IDD performs as " → BUS FREE."
→BUS FREE		:	The IDD enters a BUS FREE phase without sending a DISCONNECT or TASK COMPLETE message.
–		:	Improbable combination

Table 3.1 Retry procedure for SCSI error

Error Condition		LUN	Termination procedure	
			Status	Sense data
Parity error in MESSAGE OUT phase		I	CHECK	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
Parity error in COMMAND phase		I	CHECK	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
Parity error in DATA OUT phase		I	CHECK	ABORTED COMMAND
INITIATOR DETECTED ERROR message reception		I	CHECK	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
MESSAGE PARITY ERROR message reception (follows MESSAGE IN phase)		I	CHECK	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
MESSAGE PARITY ERROR message reception (follows other phase)		I	→BUS FREE	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
Rejected Message	TASK COMPLETE	I	→BUS FREE	NO SENSE
	DISCONNECT	I	Continues the command execution without disconnection	
	IDENTIFY	I	→BUS FREE	ABORTED COMMAND
	LINKED TASK COMPLETE (WITH FLAG)	I	→BUS FREE	ABORTED COMMAND
	MESSAGE REJECT	I	CHECK	ABORTED COMMAND
		N	→BUS FREE	NO SENSE
	RESTORE POINTERS	I	CHECK	BASED ON ORIGINAL ERROR
	SAVE DATA POINTER	I	Continues the command execution without disconnection	
	SIMPLE	I	→BUS FREE	ABORTED COMMAND
	SYNCHRONOUS DATA TRANSFER REQUEST	X	Sets data transfer mode to asynchronous mode and continues the command execution	
	WIDE DATA TRANSFER REQUEST	X	Sets wide transfer mode to 8-bit transfer mode and continues command execution	
	PARALLEL PROTOCOL REQUEST	X	Sends the MESSAGE REJECT message, sets wide transfer mode to 8-bit transfer mode, sets data transfer mode to asynchronous mode and continues the command execution.	
	IGNORE WIDE RESIDUE	I	→BUS FREE	ABORTED COMMAND
Timeout in RESELECTION phase		I	→BUS FREE	ABORTED COMMAND
Internal Controller error		I	CHECK	HARDWARE ERROR
		N	→BUS FREE	NO SENSE

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Glossary

Bus condition: Asynchronous operation condition used for status transition of SCSI bus. There are two types of bus conditions: ATTENTION and RESET conditions.

Bus phase: The name of SCSI bus state. The SCSI bus can be either in the BUS FREE, ARBITRATION, SELECTION, RESELECTION or INFORMATION TRANSFER phase. The INFORMATION TRANSFER phase is divided into subphases such as DATA IN, DATA OUT, COMMAND, STATUS, MESSAGE IN, and MESSAGE OUT.

Initiator (INIT): An SCSI device which has started up an I/O operation on the SCSI bus. The device is referred to as INIT in this manual.

CCS: The standard SCSI logical specifications developed by the ANSI working committee. The CCS defines the functions required for direct access devices (such as disk drive).

CDB: A group of data which describes the I/O operation commands. The CDB is sent from the initiator to the target.

Command: An I/O operation command to the target unit (or TARG). It is referred to as the CDB.

Disconnect: Operation performed by the target to free itself from the SCSI bus and the initiator temporarily when SCSI bus operation becomes unnecessary during command processing.

Initiator: SCSI device that has initiated an input/output operation on the SCSI device. This can be abbreviated as INIT.

Logical unit: Simple unit of equipment that can be directed to perform one I/O operation on the SCSI bus.

LUN: Logical unit number used to identify a logical unit.

LUT: A logically assigned unit which can perform I/O operations on the SCSI bus.

Message: Information that controls a series of bus phases and I/O sequence between the initiator and the target on the SCSI bus.

Reconnect: Operation performed by the target to reconnect itself with the initiator when operation on the SCSI bus becomes necessary after disconnection.

SCSI: The standard I/O interface developed by the ANSI (X3.131-1986).

SCSI ID: A physical device address which identifies an SCSI device on the SCSI bus. Each SCSI device must have a unique ID. The SCSI IDs can be 0 to 7, which corresponds to one bit of the data bus.

SCSI unit: Generic name of a unit (input/output unit, I/O controller, or host adapter) connected to the SCSI bus.

Sense code: One-byte of code attached to sense data identify the type of the detected error.

Sense data: Detailed information created by the target when any error is involved in the command termination status. This information is transferred to report the error.

Sense key: Four-bit code attached to sense data to identify the class of the detected error.

Status: One byte of information that is transferred from a target to an initiator on termination of each command to indicate the command termination status.

Target: SCSI device which performs I/O initiated by an initiator. It can be abbreviated as TARG.

Abbreviation

A

ACK	ACKnowledge
ATN	ATenTion
AWG	American Wire Gauge

B

BSY	BuSY

C

C/D	Control/Data
CCS	Common Command Set
CDB	Command Descriptor Block

D

DB	Data Bus
DBP	Data Bus Parity
DC	Direct Current
DT	Double Transfer

E

EIA	Engineering Industries Association

G

GND	GrouND

I

I/O	Input/Output
ID	IDentifier
IDD	Intelligent Disk Drive
INIT	INITiator
ISO	International Standardization Organization

L

LSB	Least Significant Byte
LUN	Logical Unit Number
LVD	Low-Voltage Differential

M

MSB	Most Significant Byte
MSG	MeSeaGe

O

OEM	Original Equipment Manufacturer

P

PPR	Parallel Protocol Request

R

REQ	REQuest
RST	ReSeT

S

SCSI	Small Computer System Interface
SDTR	Synchronous Data Transfer Request
SE	Single-Ended
SEL	SELect
ST	Single Transfer

T

TARG	TARGet
TRM	TeRMinator

W

WDTR	Wide Data Transfer Request

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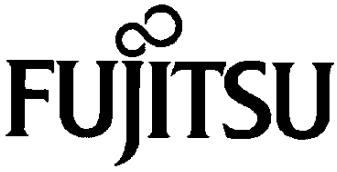
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